

REPORT DOCUMENTATION PAGE				Form Approved OMB No. 0704-0188	
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1. REPORT DATE (DD-MM-YYYY) 10-01-2006		2. REPORT TYPE Final Technical Report		3. DATES COVERED (From - To) Jul 2003 - Dec 2005	
4. TITLE AND SUBTITLE Towards a Fully Modular Power System Architecture for DC-DC Converters				5a. CONTRACT NUMBER	
				5b. GRANT NUMBER N00014-03-1-0802	
				5c. PROGRAM ELEMENT NUMBER	
6. AUTHOR(S) Ayyanar, Raja Ledezma, Enrique				5d. PROJECT NUMBER	
				5e. TASK NUMBER	
				5f. WORK UNIT NUMBER	
7. PERFORMING ORGANIZATION NAME(S) AND ADDRESS(ES) Arizona Board of Regents acting for and on behalf of Arizona State University Office for Research and Sponsored Projects Administration (ORSPA) PO Box 873503 Tempe, AZ 85287-3503				8. PERFORMING ORGANIZATION REPORT NUMBER DWA0092/TE	
9. SPONSORING/MONITORING AGENCY NAME(S) AND ADDRESS(ES) Office of Naval Research 875 N. Randolph Street One Liberty Center Arlington, VA 22203-1995				10. SPONSOR/MONITOR'S ACRONYM(S) ONR	
				11. SPONSOR/MONITOR'S REPORT NUMBER(S)	
12. DISTRIBUTION/AVAILABILITY STATEMENT Unclassified and unlimited for public distribution					
13. SUPPLEMENTARY NOTES					
14. ABSTRACT Fully modular power system architecture for dc-dc conversion, where low-power, low-voltage (input and output) building block dc-dc converters can be connected in any combination of series/parallel configurations at the output and/or at the input sides, has several advantages including increased reliability, standardization of design and components, higher power density and efficiency. An important component of such architecture is the autonomous, input series configuration with active input voltage and load current sharing, towards which this research project has made significant contributions. The major research tasks accomplished in this project are: 1. Development of control methods for input-series and output-series (ISOS) configuration with active voltage sharing; 2. Development of input-voltage share bus scheme for input-series, output parallel (ISOP) connection that makes the converter modules self-contained and identical, leading to fault tolerant capability; 3. Study on magnetic approaches to input-voltage sharing for input-series connected converters; and 4. development of interleaving techniques for input series connected					
15. SUBJECT TERMS modular power system, dc-dc converters, input series, ISOP, ISOS, input voltage sharing, load sharing, autonomous control, democratic input sharing, automatic master slave control, magnetic sharing, interleaving					
16. SECURITY CLASSIFICATION OF:			17. LIMITATION OF ABSTRACT	18. NUMBER OF PAGES	19a. NAME OF RESPONSIBLE PERSON
a. REPORT	b. ABSTRACT	c. THIS PAGE			Avery Wright, Sponsored Projects Ofcr, ORSPA
U	U	U	UU	79	19b. TELEPHONE NUMBER (Include area code) 480.727.7983

Final Report

**Towards a Fully Modular Power System
Architecture for DC-DC Converters**

ONR Award Number: N00014-03-1-0802

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January 2006

EXECUTIVE SUMMARY

Fully modular power system architecture for dc-dc conversion, where low-power, low-voltage (input and output) building block dc-dc converters can be connected in any combination of series/parallel configurations at the output and/or at the input sides, has several advantages including increased reliability, standardization of design and components, higher power density and efficiency. An important component of such architecture is the *autonomous, input series* configuration with active input voltage and load current sharing, towards which this research project has made significant contributions. The major research tasks taken up in this project are:

1. Development of control methods for input-series and output-series (ISOS) configuration
2. Development of *input-voltage share bus scheme* for input-series, output parallel (ISOP) connection that makes the converter modules *self-contained and identical* leading to fault tolerant capability.
3. Study on magnetic approaches to input-voltage sharing for input-series connected converters
4. Investigations on interleaving techniques to reduce filter requirement.

A three-loop control scheme has been developed for the ISOS configuration, which ensures input and output voltage sharing under dynamic and steady state conditions. The dynamic input voltage reference for the input voltage loop achieves minimum interactions among the different converters and among different control loops. Design procedure based incremental negative resistance model has been developed. The proposed ISOS scheme has been validated on a three-converter hardware prototype.

Two schemes using input voltage share bus, namely democratic input voltage share scheme and automatic master-slave scheme, have been developed to realize autonomous ISOP configuration using self-contained and identical modules. Each of the converter modules has its own dedicated output voltage loop whose reference is modified based on the error in input voltage sharing. It has been found that for voltage mode control, mismatch in the output voltage reference among the modules is the critical parameter. The input voltage correction loop compensates for this mismatch. Design methods to choose the gain of the input voltage controller have been developed. The analysis and design methods have been validated on a two-converter hardware prototype.

The possibility of input-voltage sharing in series connected converters through magnetic coupling has been explored. A possible scheme where a dedicated balance winding in the power transformer of each converter is connected in a daisy-chain fashion to the following converter through diodes is proposed. This scheme ensures input voltage sharing provided the leakage inductance and the value of the input filter capacitance are small. However, for practical values of leakage inductance and input filter

capacitor the scheme is not very effective. Control based approaches are found to be superior to the magnetic approach.

An important advantage of series/parallel connection of modular converters is the reduction of filter requirement through interleaving of the converter modules. Interleaving refers to suitable phase shifting of the gate drive signals of the modules such that there is significant cancellation of ripple in the input/output currents and/or voltages. This project has investigated interleaving techniques for input series configurations. For the ISOP configuration, interleaving at the output end (parallel connection) is identical to that of the conventional IPOP converters. At the series connected input side also the optimal phase shift is $360^\circ/n$. At the input side, the current through the input capacitor of each module is similar to that of a stand-alone converter, and hence, there is no savings in the ratings of the input filter capacitor. However, the ripple voltages in the filter capacitors (which appear as the ripple voltage across the input inductor) cancel due to interleaving, leading to *significant* savings in the input inductor. The frequency of the ripple in the input current is scaled up by the number of converters, n . The savings in the filter requirement for various values of ' n ' and duty ratio has been derived.

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1. INTRODUCTION

A fully modular power system architecture is envisioned for dc-dc power conversion. In such an architecture, low-power, low-voltage (input and output) building block dc-dc converters can be connected in any combination, series or parallel, both at the output *as well as at the input* sides, to realize any input-output specifications. Fig. 1 illustrates an example of a 5 kW power supply system operating from a 1000 V dc source and delivering a well regulated output voltage of 50 V at a maximum load current of 100 A. This system is implemented using a total of twenty 250 W power supplies, each with an input voltage rating of 100 V, and providing a regulated 25 V output at a maximum current of 10A. (Though not shown in the figure, required level of redundancy may also be included).

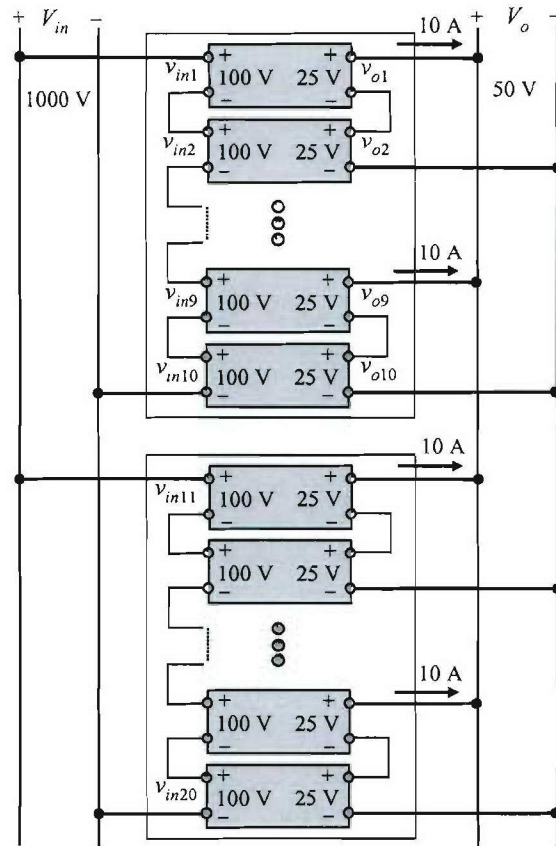


Fig. 1. Example of a fully modular power system architecture for dc-dc conversion

The main advantages of the modular approach include:

- Significant improvement in reliability by introducing desired level of redundancy [1-5]
- Standardization of components leading to reduction in manufacturing cost and time
- Power systems can be easily reconfigured to support varying input-output specifications
- Possibly higher efficiency and power density of the overall system, especially with interleaving.

Fig. 2 shows the four possible combinations of input-output connections. Among these combinations, the input-parallel and output-series (IPOS) connection is well known and is presently used in many applications requiring high output voltages. Standard dc-dc converters, with independent output voltage controllers, can be connected in series at the output achieving equal sharing of output voltage and input current. However, in order to obtain the advantages of modularity such as redundancy, a common output voltage loop or an output-voltage share bus is required. A scheme based on common output voltage loop and individual inner current loops is discussed in [5].

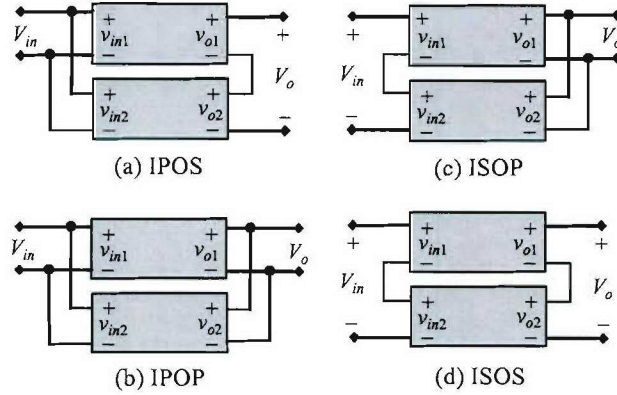


Fig. 2. Four possible combinations of input-output connections.

(a) input parallel and output series, (b) input parallel and output parallel, (c) input series and output series and (d) input series and output series

The input-parallel and output-parallel (IPOP) connection has been the subject of vigorous research recently, fueled by the requirement of low voltage and very high current outputs. The

challenge here is to ensure equal sharing of load current (hence, input currents also) among the modular converters, in spite of small differences in the power stage and control parameters of the different converters, and finite differences in the impedances of interconnections. Several control schemes, such as many droop schemes [6], [7], [8], master-slave scheme [9], [10], democratic current share scheme [11]-[13], and frequency based current share scheme [4], have been proposed to ensure active load current sharing among the parallel converters. Paralleling techniques that do not require direct interconnection of control circuits of the various modules have also been investigated [14]. An excellent review and comparison of different methods for IPOP connection are given in [15].

1.1 Advantages of input-series connections

The ability to connect converters in parallel or series only at the output does not result in complete modularity. Given the wide variety of input sources possible, such as rectified utility voltage, batteries and fuel cells, the input voltage to a system can also vary widely for different applications. Hence, it is essential to develop converters that can be connected in series at the input (Figs. 2c and 2d) also, with dynamic input-voltage sharing capability.

Apart from considerations of modularity, the input-series connection has many other advantages such as:

- Enables use of MOSFETs with low voltage rating, which are optimized for very low $R_{DS\ ON}$, leading to higher efficiency. At higher voltages, the $R_{DS\ ON}$ of a MOSFET depends mainly on the drift region resistance, which is roughly proportional to $BV_{DSS}^{2.6}$, where BV_{DSS} is the break down voltage of the MOSFET [16]. Hence, ‘ N ’ MOSFETs each with a voltage rating of $\frac{BV_{DSS}}{N}$, have a combined $R_{DS\ ON}$ which is significantly lower than the $R_{DS\ ON}$ of a single MOSFET with a voltage rating of BV_{DSS} .
- MOSFETs can be used instead of IGBTs for high input-voltage applications. Hence, switching frequency, and therefore, power density of such systems can be increased.

- Input-series and output-parallel connection leads to smaller conversion ratios for the individual converters, especially for the popular low output voltage applications. This leads to more efficient power conversion [5].
- Possibility of interleaving to reduce filter ratings and improve transient performance (similar to input-parallel converters)

A main trend in switch mode power supplies is the requirement of very low output voltages with very high currents. With the proposed ISOP connection for such applications, the conversion ratio for each converter, and therefore, the turns-ratio of the power transformer, is much smaller. This can result in smaller leakage inductances and other parasitic components, thus improving efficiency. However, in spite of several advantages of input-series connection, not much research has been reported on this configuration. In [17], input-series and output-parallel (ISOP) connection has been implemented for a two-converter system, using a charge control scheme with input voltage feed forward. In an earlier ONR supported research, the authors have developed three different control schemes for the ISOP configuration [18-20].

Direct series connection of devices such as MOSFETs and IGBTs for high input voltage applications has also been investigated [21]. However, the advantages of modularity such as scaling and reconfiguration, as well as interleaving to reduce filter requirement, are easily achieved in series connected converter modules, than in series power devices.

1.2 Prior work on input-series and output-parallel (ISOP) systems

Prior ONR sponsored research work has established the feasibility of the basic ISOP configuration, even with finite differences in various converter parameters. The feasibility of the ISOP connection can be verified by considering power balance in individual converters, under steady state. Fig. 3 shows a numerical example of how input voltage as well as output current can be shared equally, in the presence of parameter mismatches such as different turns-ratios for the power transformers. Under steady state, the input currents of the two converters are equal due to the series connection. If the input voltages are also maintained equal *by control*, then the input powers of the two converters are equal. Therefore, by power balance (neglecting losses), the output powers of the two converters are equal. Since, the parallel connection at the output ensures that the output voltages are equal, the output currents are also automatically made

equal. If the parameters of the two converters are identical, the duty ratios will be equal; for any mismatch in the parameters such as turns-ratio of the transformer, the duty ratios will differ to correct for the mismatch, as illustrated in Fig. 3. It should be noted, however, that the above discussion assumes that the converters operate stably in steady state. The necessary condition for stable operation is discussed in the following sections.

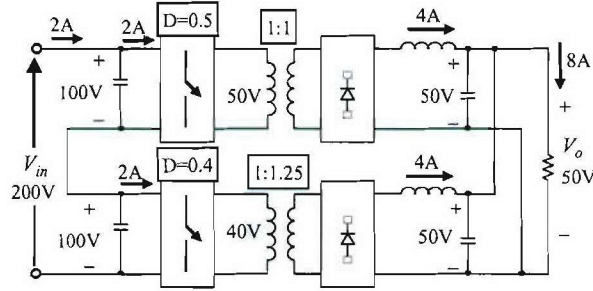


Fig. 3. Feasibility of input voltage *and* output current sharing with mismatch in transformer turns-ratio.

1.2.1 Need for input voltage controller

It is easy to appreciate that standard converters without any special input voltage or load current sharing controllers, when connected in ISOP combination, will not result in stable operation. This is similar to the case of the widely used IPOP connection, where, in the absence of a load current sharing controller, even a small mismatch in parameters can lead to wide variations in the individual output currents of the converters.

For the ISOP connection, it is important to note that *even with load current sharing controllers*, similar to those used in IPOP connection, stable operation is *not* achieved. For example, consider again the ISOP connection shown in Fig. 3, and assume that the system has an output current sharing controller. If the input voltage of converter 1, for example, increases slightly due to a disturbance, the output current sharing controller reduces the duty ratio of this converter, in order to maintain its current equal to that of the converter 2. This reduces the average input current drawn by converter 1, leading to further increase in its input voltage. This process leads to a runaway condition, resulting in large voltage stress across converter 1, eventually destroying it.

Fig. 4 shows the simulated waveforms corresponding to an ISOP connection with a load-current-share mechanism, but *without* an input-voltage controller. The two series connected converters use current mode control, with a common output voltage loop providing the current reference to both converters. As seen in Fig. 4, in spite of the common current reference, the input voltages diverge. Hence, a dedicated input voltage control loop, which adjusts the duty ratios of the individual converters depending on the error in input voltage sharing, is required. It may be noted that input voltage sharing automatically ensures output load current sharing, without the need for a dedicated load current share controller.

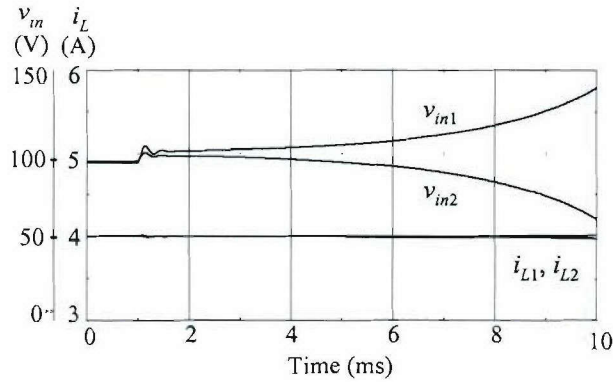


Fig. 4. Divergence of input voltages in ISOP system with current mode control and without input voltage control.

Two different control schemes which ensure sharing of input voltage and load current have been developed in the prior work as briefly explained below.

1.2.2 Three loop, dynamic input voltage reference control scheme for ISOP configuration

Fig. 5 shows the three-loop, dynamic input voltage reference scheme for ISOP connection of N forward converters (the reset windings for the transformer are not shown, for clarity). As seen, the scheme consists of three control loops to ensure equal input voltage and load current sharing. A single output voltage loop, which is common to all the converters, provides the initial current reference, i'_{ref} to all the individual, inner current loops. The compensator for the output voltage loop is denoted as G_{V_o} . Each converter also has an individual input voltage loop, which adjusts the above current reference to its inner current loop, based on the error between the reference input voltage and the actual input voltage of the particular

converter. The inner current loop can be of either peak current mode or average current mode with a compensator G_{I_j} as shown in Fig. 5. The inner current loop controls the duty ratio of the converter such that the output inductor current equals the adjusted current reference, referred to as i_{ref} .

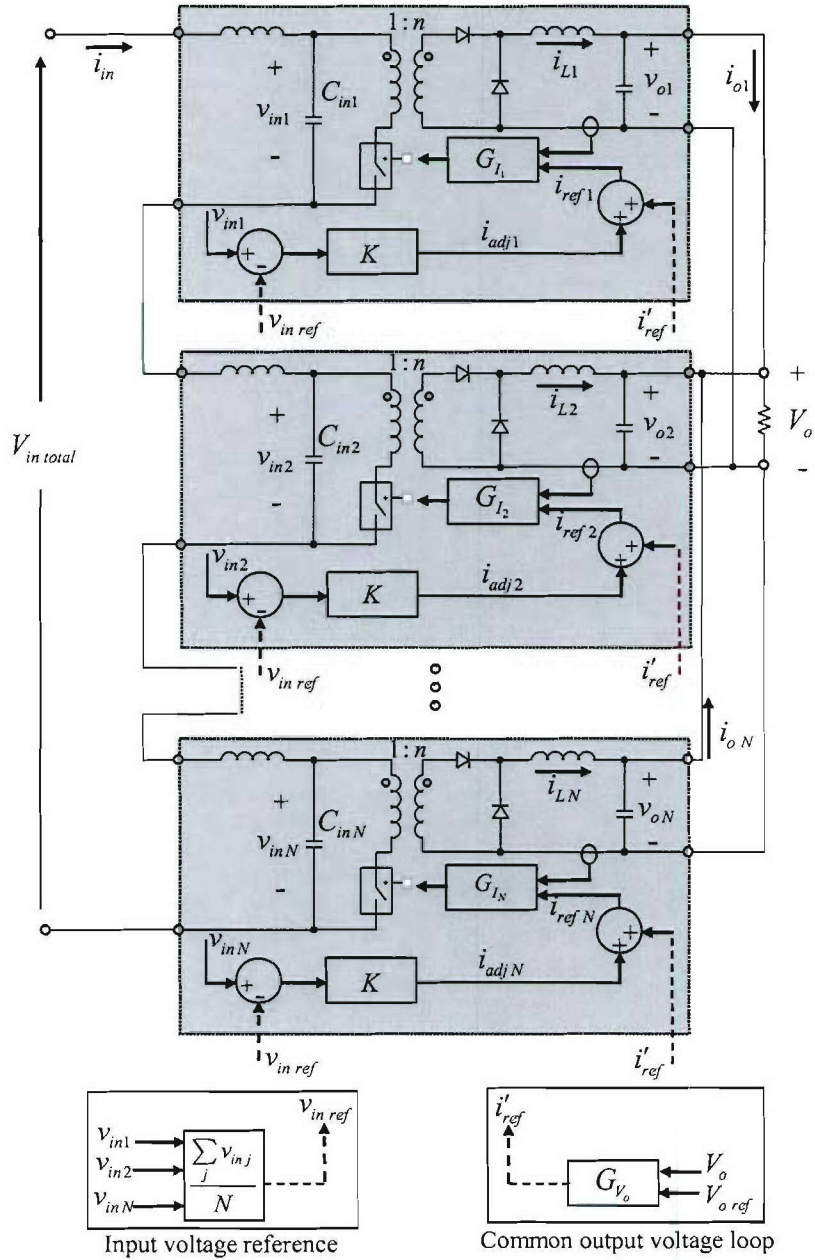


Fig. 5. Three-loop control scheme with dynamic input voltage reference for ISOP connection.

The input voltage reference is chosen to be the average of all the converter input voltages, as given in (1). Note that the converter input voltage is defined as the voltage across the input capacitor of the corresponding converter. It takes into account the resonance due to the input LC filter. In particular, the sum of the converter input voltages (capacitor voltages) is not dynamically equal to the total system input voltage, $v_{in\ total}$.

$$v_{in\ ref} = \frac{\sum_{j=1}^N v_{in\ j}}{N} \quad (1)$$

Other possible references for the input voltage loop are $\frac{v_{in\ total}}{N}$ and a constant reference. The main advantages of the dynamic input voltage reference are that it minimizes the interaction among the different control loops and results in better transient performance. The three loop scheme has been validated on a two-converter experimental prototype [18].

1.2.3 Common duty ratio scheme for ISOP configuration

The common duty ratio scheme is a very simple control method for the ISOP connection, which does not require input-voltage or load-current share loop, but still ensures equal sharing of input voltage and load current. It relies on the inherent, self-correcting mechanism of input-series and output- parallel connection when the duty ratio of all the converters is made common. This scheme does not result in perfectly equal sharing [18, 20]. The sharing is different to the extent that the turns-ratios of the power transformers and other parameters in the individual converters are different. However, with modern transformer manufacturing techniques such as planar transformers with precise printed circuit board windings, the mismatch in turns-ratios, and hence, mismatch in input-voltage and load-current sharing can be made negligible. The main advantage of the proposed scheme is that neither input voltage nor output current (if current mode control is not used) needs to be sensed, leading to extremely simple implementation of a fully modular architecture.

The schematic of the proposed common duty ratio scheme for the ISOP configuration consisting of ‘N’ forward converters is shown in Fig. 6. In this implementation, the converter N is the ‘master’ converter and all the other converters are ‘slave’ converters. A single output

voltage loop generates the current reference for the inner current loop of the master converter N . A peak or average mode current controller in the ‘master’ converter generates suitable duty ratio, d , such that its output inductor current, i_{L_N} , equals the above current reference. This duty ratio, d , is made common to all the other converters too. If interleaving of the converters is not required, then the actual gate switching signal (with suitable isolation) itself can be made common to all the converters. If interleaving is desired, then the duty ratio signal can be shared, which will then be compared with suitably phase-shifted ramp signals in the individual converters to generate the individual gate drive.

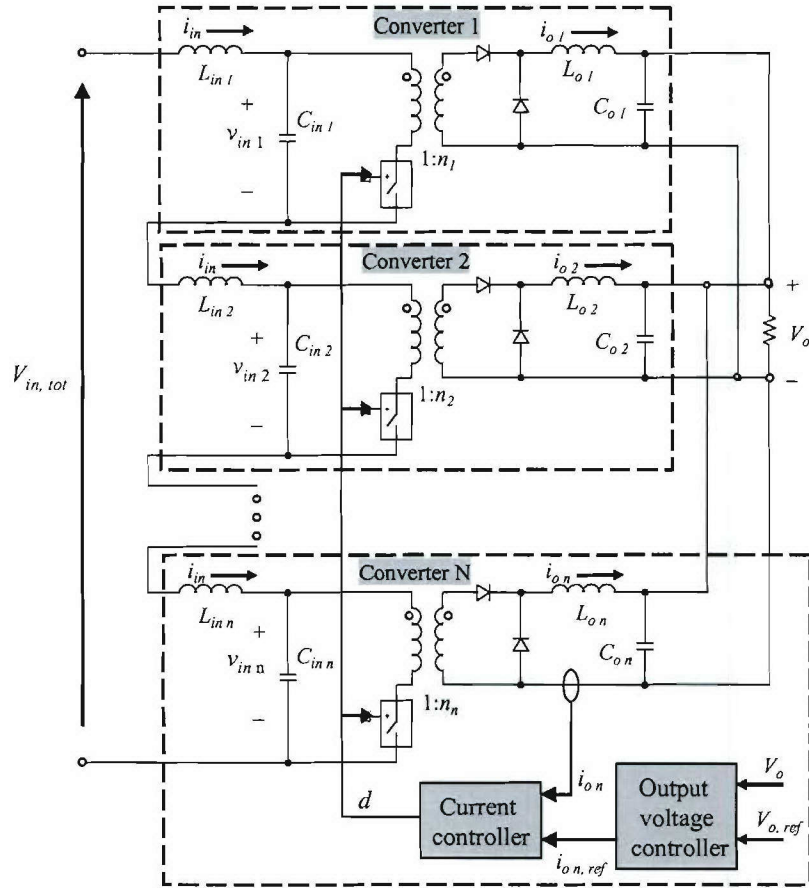


Fig. 6. Common duty ratio control scheme for ISOP connection.

In the ISOP connection with common duty ratio control, the converter with higher turns-ratio and hence higher average rectified voltage tends to produce a higher output inductor

current. However, this leads to a higher input current in this converter, which discharges the input capacitor and reduces the input voltage of the corresponding converter. Hence, the average secondary voltages of all the converters become equal. The primary side voltages are then given by the product of the turns-ratio and the equal secondary side voltages. This self-correcting mechanism ensures stable operation, and the input voltage and load current are shared equally to the extent that the transformer turns-ratios are equal.

1.3 Objectives and scope of the research

Referring to Fig. 2, among the possible combinations of connections, the input-series and output series (ISOS) connection has not been explored so far. An objective of this project is to investigate this configuration and develop suitable control schemes to ensure equal sharing of input and output voltages among the modules. The ISOS configuration is required for a fully modular dc-dc power system architecture and is especially useful when both the input and output voltages are high.

All the schemes described above for the input-series, output-parallel (ISOP) connection require an output voltage control loop *common* to the ‘n’ converters. Hence, the individual modules are not self-contained, and are not identical, leading to degradation of modularity and reliability [15, 22]. Hence, a main objective of this research project is to develop identical and self-contained modules to realize a fully modular power system architecture. The approach is to provide the required output voltage control loop in *each of the converters*, thus making the modules self-contained and eliminating the need for any external control blocks. Active input voltage sharing and automatic load current sharing are achieved using a novel **“input voltage share bus”** concept, inspired by the ‘load share bus’ concept [10-13] used in conventional parallel-input, parallel-output connection.

Apart from the control-based schemes discussed above, it is possible to achieve input-voltage sharing in series connected converters through magnetic means. An objective of the proposed research is to study the different magnetic means of achieving input voltage and load sharing, and compare them with the control-based approaches for performance in terms of sharing, control complexity, electro magnetic interference (EMI) and switch ratings.

A main advantage of series/parallel connection of modular converters, apart from standardization and reliability through redundancy, is the reduction of filter requirement through

interleaving of the converter modules. Interleaving refers to suitable phase shifting of the gate drive signals of the modules such that there is significant cancellation of ripple in the input/output currents and/or voltages. Interleaving techniques for the parallel connections have been well studied [23]. Hence, an objective of this research is to investigate interleaving techniques for input series configurations and quantify its benefits.

The major tasks of the research are as follows:

1. Development of *input-voltage share bus scheme* for input-series, output parallel connection, that makes each of the modules *self-contained* and eliminates the need for external control blocks as required in the previous work
2. Development of control methods for series-input, series-output connection, a combination that has not been explored so far.
3. Study on magnetic approaches to input-voltage sharing for input-series connected converters
4. Investigations on interleaving among the modular converters to reduce filter requirement, and to improve dynamic performance.

2. NEGATIVE RESISTANCE BASED ANALYSIS OF INPUT SERIES CONVERTERS

This section discusses a simple model for the ISOP configured system when each of the converter modules employs current mode control. Based on this model, expression for the minimum gain of the input voltage controller is derived. For the purpose of analyzing the stability and performance of the input voltage loop, each converter can be modeled as an equivalent *incremental* negative resistance as seen from the terminals of the input capacitor. The incremental negative resistance model of a dc-dc converter is discussed in detail, especially in the context of designing input filters and understanding their effects on the stability of the overall system, in [24] and [25]. Regardless of whether current-mode control or voltage-mode control is employed, the input terminals of a stand alone converter exhibits negative resistance characteristics, since a positive incremental change in input voltage results in a proportionate, but negative incremental change in the input current. For current-mode controlled converters, the frequency range extends up to the bandwidth of the inner current loop. A more accurate model for the converter is a negative resistance in parallel with a capacitance, C that depends on the above bandwidths [24]. However, since the bandwidth of the current loop is much higher than that of the input voltage loop here, the parallel capacitance is neglected.

2.1 Equivalent circuit based on negative resistance model

Fig. 7 shows the equivalent circuit used to analyze the N converter ISOP system. Each converter is modeled as an equivalent negative resistance, R_{neg} , connected to an input LC filter. In the actual system, the input voltage loop adjusts the reference to the output inductor current. The inductor current follows the reference with a small but finite response time, which together with the change in duty ratio translates into a change in the input current. The dynamics of the input current depend on the bandwidth of the inductor current loop and dynamic changes in the duty-ratio, d . In the equivalent circuit of Fig. 7, the correction mechanism is modeled as an ideal current source, $i_{adj} = K(v_{inj} - v_{inref})$, connected directly across the input capacitor of each converter. After the scaling factors due to transformer turns-ratio and the steady-state duty ratio, D , are taken into account, this is a valid, close approximation at frequencies less than the bandwidth of the inner current loop, *and* when the magnitude of the correction currents at the input is relatively small. The validity of the equivalent circuit is confirmed by the excellent

matching of simulation results obtained using the above equivalent circuit representation and those corresponding to the full circuit model as discussed later in Section 2.3.

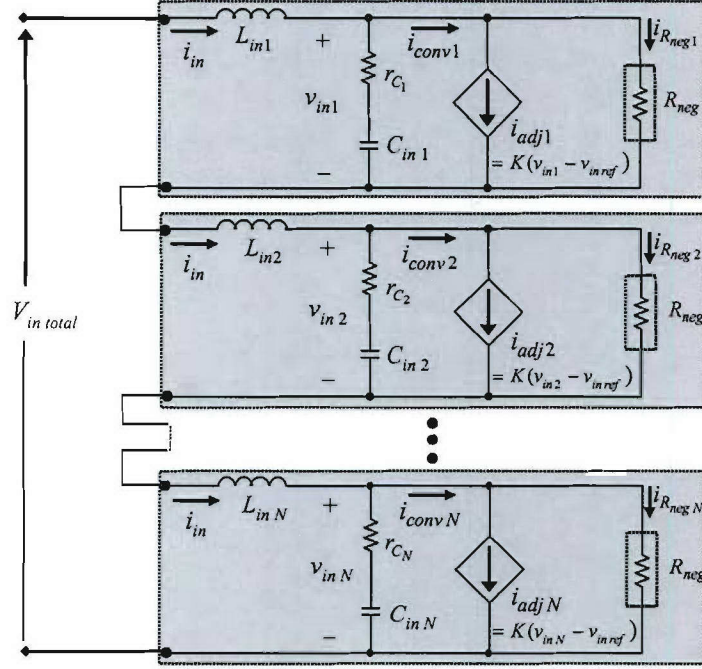


Fig. 7. Equivalent circuit based on negative resistance model for an N -converter ISOP system.

The value of the incremental negative resistance, R_{neg} of the converter depends on the operating load and input voltage. While analyzing the stability of the system with input voltage control, the worst-case condition is the maximum load current and minimum input voltage. Hence, the value of the negative resistance used in the model of Fig. 7 is as given in (2).

$$R_{neg} = - \frac{V_{in \min}^2}{P_{o \max}} \quad (2)$$

where, $V_{in \min}$ is the minimum specified input voltage to an individual converter, and $P_{o \max}$ is the maximum output power of an individual converter.

2.2 Derivation of stabilizing controller gain

Referring to Fig. 7, let us define the following.

$$v_{in \text{ sum}} = \sum_{j=1}^N v_{in j} \quad (3a)$$

$$v_{in ref} = v_{in avg} = \frac{v_{in sum}}{N} \quad (3b)$$

$$i_{adj j} = K(v_{in j} - v_{in avg}) \quad (3c)$$

where, K is the constant gain of the input voltage controller.

The objective is to maintain the input voltages, as seen at the input capacitor terminals, of all the converters equal to each other, and therefore, equal to $v_{in avg}$. The necessary condition for stability of the system shown in Fig. 7, is that for an **increase** in any converter input voltage, for example, v_{in1} , relative to the average input voltage, $v_{in avg}$, the input current drawn by the converter, i_{conv1} (which is the sum of the current through the negative resistance model and the correction current) should **increase**, relative to the average of the input currents drawn by all the converters, $i_{conv avg}$, which is equal to $\sum_{j=1}^N i_{conv j}$. This ensures that the higher input current discharges C_{in1} appropriately to reduce v_{in1} .

In terms of ac perturbation quantities, the condition is that $\tilde{v}_{in j} - \tilde{v}_{in avg}$ should be in phase with $\tilde{i}_{conv j} - \tilde{i}_{conv avg}$. Note that for ac analysis,

$$\tilde{i}_{R_{neg j}} = \frac{\tilde{v}_{in j}}{R_{neg}} \quad (4)$$

where, R_{neg} has a negative value given in (2). Also, the equivalent incremental negative resistance of each converter is assumed equal. From Fig. 6,

$$\begin{aligned} \tilde{i}_{conv1} &= K(\tilde{v}_{in1} - \tilde{v}_{in avg}) + \frac{\tilde{v}_{in1}}{R_{neg}} \\ \tilde{i}_{conv2} &= K(\tilde{v}_{in2} - \tilde{v}_{in avg}) + \frac{\tilde{v}_{in2}}{R_{neg}} \\ &\dots \\ \tilde{i}_{convN} &= K(\tilde{v}_{inN} - \tilde{v}_{in avg}) + \frac{\tilde{v}_{inN}}{R_{neg}} \end{aligned} \quad (5)$$

Adding the expressions in (5),

$$\tilde{i}_{conv avg} = \frac{\sum_{j=1}^N \tilde{i}_{conv j}}{N} = \frac{K \sum_{j=1}^N \tilde{v}_{in j} - K \tilde{v}_{in sum}}{N} + \frac{\sum_{j=1}^N \tilde{v}_{in j}}{N R_{neg}} = \frac{\tilde{v}_{in avg}}{R_{neg}} \quad (6)$$

From (5) and (6),

$$\begin{aligned} \tilde{i}_{conv 1} - \tilde{i}_{conv avg} &= K(\tilde{v}_{in 1} - \tilde{v}_{in avg}) + \frac{1}{R_{neg}}(\tilde{v}_{in 1} - \tilde{v}_{in avg}) \\ &= (\tilde{v}_{in 1} - \tilde{v}_{in avg}) \left[K + \frac{1}{R_{neg}} \right] \end{aligned} \quad (7)$$

For stable operation, $\tilde{i}_{conv 1} - \tilde{i}_{conv avg}$ should have the same sign as $\tilde{v}_{in 1} - \tilde{v}_{in avg}$. Therefore, the condition for stability is given by (8).

$$K > K_{\min} = \frac{1}{|R_{neg}|} \quad (8)$$

This condition for the minimum gain for the proportional input voltage controller is independent of the capacitance or ESR values of the input capacitors, and is strictly valid even if the impedances of the input capacitors of different converters are significantly different. It may be noted that while K_{\min} ensures stability, higher values of K result in faster correction in input voltages after a disturbance. However, this faster response is at the expense of increased switch currents. For the dynamic input voltage reference scheme, the value of K is limited mainly by the switch ratings. Selection of suitable K is discussed in Section 2.4.

As mentioned earlier, in the actual system input voltage differences are corrected by adjusting the output inductor currents of individual converters. The output inductor current and the actual correction current at the input are related by the turns-ratio of the power transformer, and the operating duty ratio. Considering these two scaling factors, the value of minimum gain, $K_{\min, actual}$ for stability of the actual system is given by,

$$K_{\min, actual} = \frac{1}{n D} \frac{1}{|R_{neg}|} \quad (9)$$

where, n is the turns-ratio of the power transformer, and D is the steady state duty-ratio of the converter at the given operating condition.

2.3 Validation through simulation of a two converter system

The above analysis is validated through numerical simulation of a two forward converter system connected in ISOP configuration. The two-converter system is simulated using both the negative resistance model, as well as the full large-signal average model, in PSpice. The results match very closely, validating the analysis based on the simpler negative resistance model. The PSpice schematic of the negative resistance model, similar to that of Fig. 7, is shown in Fig. 8.

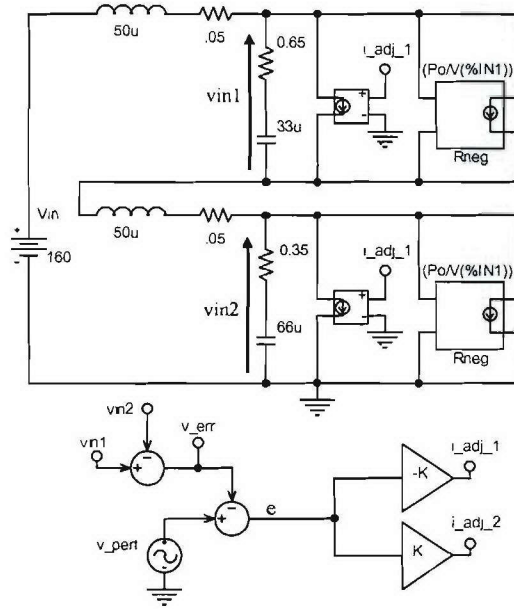


Fig. 8. PSpice schematic of a two-converter ISOP system based on negative resistance model.

The incremental negative resistance is implemented by a controlled current source whose magnitude is inversely proportional to the converter input voltage. The input capacitors are purposely made dissimilar in order to study the performance of the proposed controller.

The schematic of the detailed, large signal average model is shown in Fig. 9. The average model is obtained by replacing the PWM switch of each converter by its ideal transformer model, PWM_1 and PWM_2 . The turns-ratios of these ideal transformers are dynamically varying and are equal to the instantaneous duty-ratios, d_1 and d_2 respectively [26].

T_1 and T_2 are the power transformers of the two converters with fixed turns-ratios. There is a common output voltage loop, individual average current mode inner current loops, whose references are adjusted by individual input voltage loops. The output voltage loop compensator is designed to achieve a bandwidth of 5 kHz and the two inner average current loops are designed for a bandwidth of approximately 50 kHz. The structure of the compensators and the values used are also shown in Fig. 9.

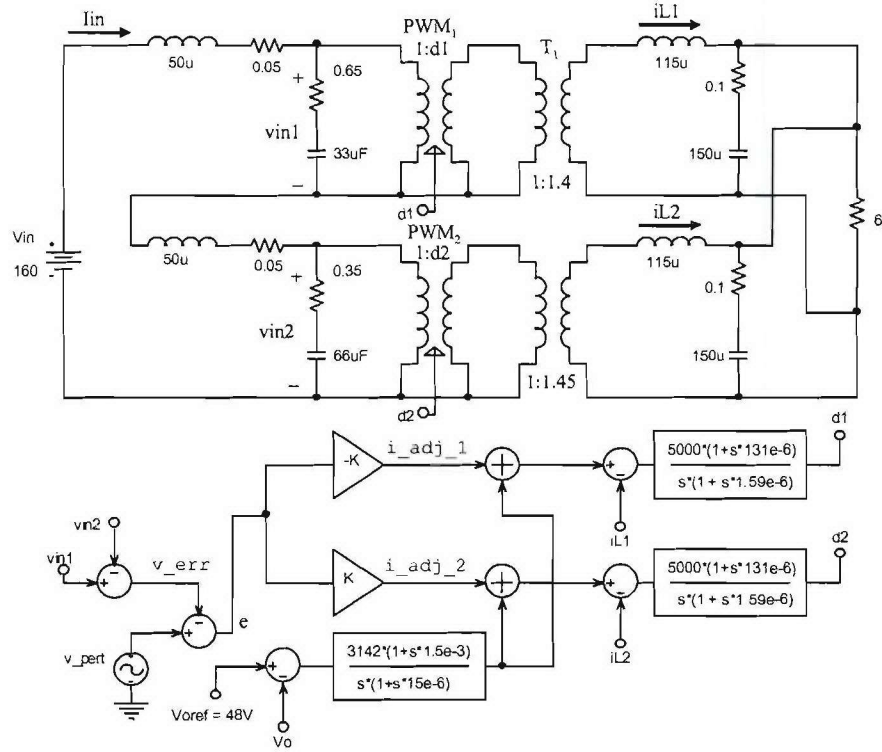


Fig. 9. PSpice schematic of a two-converter ISOP system based on full average model including different control loops.

For the two converter system,

$$v_{in1} - v_{inref} = v_{in1} - \left[\frac{v_{in1} + v_{in2}}{2} \right] = \frac{v_{in1} - v_{in2}}{2} \quad (10)$$

$$i_{adj1} = K(v_{in1} - v_{inref}) = \frac{K}{2}(v_{in1} - v_{in2}) \quad (11a)$$

$$i_{adj2} = K(v_{in2} - v_{inref}) = \frac{K}{2}(v_{in2} - v_{in1}) = -i_{adj1} \quad (11b)$$

For frequency domain simulation, in order to obtain a convenient point for signal injection, the error voltage $v_{in1} - v_{in2}$, referred to as v_{err} , is considered as the variable to be controlled, with the control reference being zero. By perturbing this reference, the frequency response plots of the two-converter system can be obtained. This scheme is illustrated in the two schematics shown in Fig. 8 and Fig. 9. In both the schematics, the open loop transfer function for the input voltage control loop is given by (12).

$$G_{OL}(s) = \frac{v_{err}(s)}{e(s)} \quad (12)$$

Fig. 10 shows the Bode plots of open loop gain $G_{OL}(s)$, obtained from both negative resistance model as well as full average model. The two models match very closely for frequencies up to 10 kHz. As seen from the plots, the open loop gain has an unstable pole (right half plane) at around 70 Hz. This pole frequency is determined by the value of input capacitance and the magnitude of the incremental negative resistance of the converter.

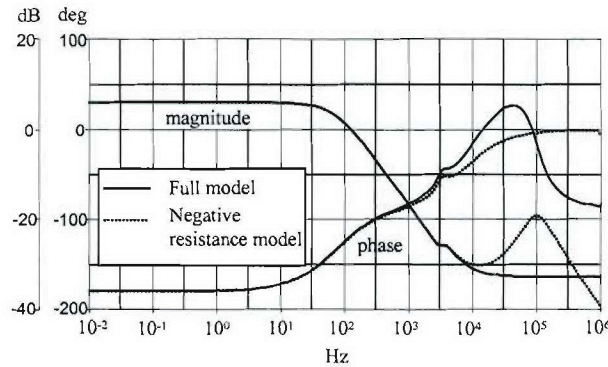


Fig. 10. Open loop gain of the input voltage loop.

The gain, K of the input voltage controller should be chosen such that the closed loop gain $G_{CL}(s)$ defined in (13) is stable.

$$G_{CL}(s) = \frac{v_{err}(s)}{v_{pert}(s)} \quad (13)$$

Fig. 11 shows the Bode plots of closed loop gain, $G_{CL}(s)$ for different values of K . As seen from Fig. 10, for $K < K_{\min}$, the system is unstable, since the closed loop transfer function has an unstable pole (at around 20 Hz for this particular value of K , where the magnitude drops at a rate of -20dB/decade while the phase increases). For $K > K_{\min}$, the system is stable, as seen from Fig. 11 (darker plots), thus validating the stability conditions given in (8) and (9).

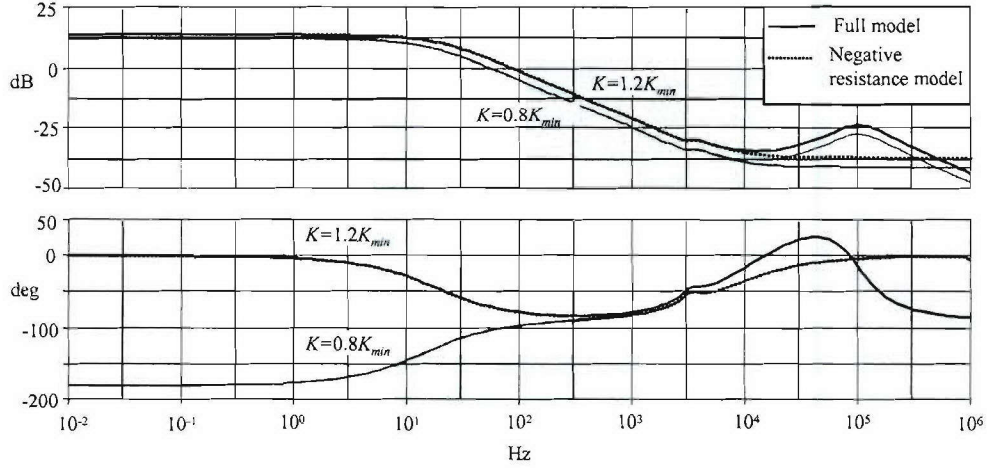


Fig. 11. Closed loop Bode plot for the input voltage loop corresponding to stable and unstable values for gain, K .

The input voltage control loop has to correct for unbalances in the individual converter input voltages caused by disturbances such as a step change in total input voltage. Hence, a main transfer function of interest for the input voltage control loop is $\frac{v_{err}(s)}{v_{in\ total}(s)}$, i.e., the response in the individual input voltages due to changes in the total system input voltage. This transfer function is obtained by keeping the reference to v_{err} as zero, and perturbing the total input voltage. The corresponding Bode plots obtained using negative resistance model and full average model are shown in Fig. 11, for three different values of K . As seen, for $K < K_{\min}$, there is an unstable pole, which is eliminated at higher values of K . Since, this is a response to disturbance input, the gain of the transfer function should be low for better disturbance rejection, which is achieved by increasing K . Also, note that at 120Hz the gain of the disturbance transfer

function is low ($< -50\text{dB}$), which implies that the proposed scheme will work well when the input dc voltage to the system is obtained by rectifying ac mains voltage.

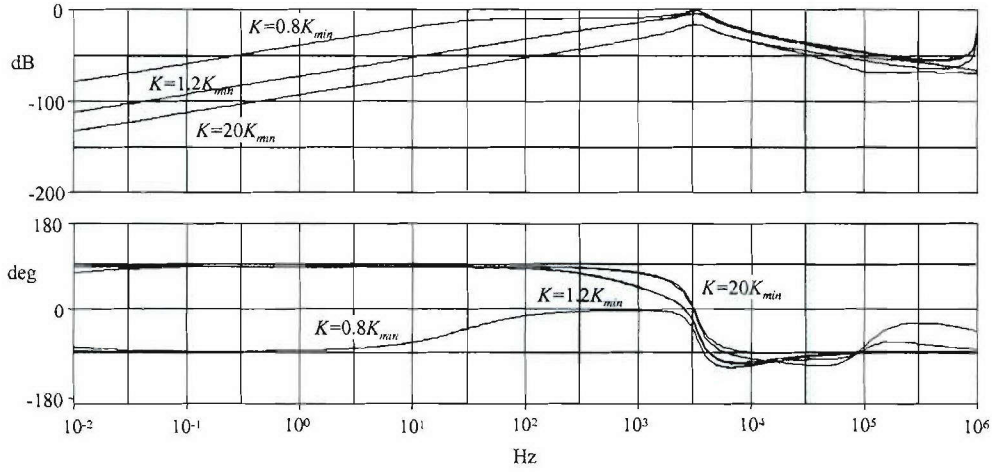


Fig. 12. Bode plots corresponding to $v_{err}(s)/v_{in\ total}(s)$ for different values of gain, K .

Fig. 13 shows the time domain response in the individual input voltages when a step change of 20 V is applied to the total system input voltage. Plots corresponding to both the negative resistance model and the full average model are shown. As seen in Fig. 13a, for $K < K_{min}$, the system is unstable, with the two converter input voltages diverging, resulting in a run-away mode. For K greater than, but close to K_{min} , the system is stable, but it takes a long time for the correction in converter input voltages, as shown in Fig. 13b. For $K \gg K_{min}$, the two converter input voltages converge quickly as seen from Fig. 13c. The oscillations in the individual input voltages in Fig. 13 are due to the resonance in the input LC filters, and do not

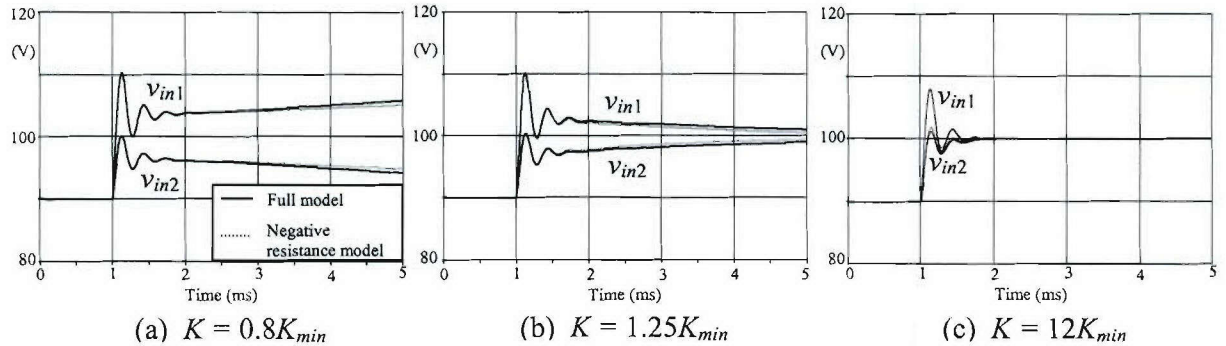


Fig. 13. Response in the individual converter input voltages to a step change of 20V in total input voltage.

reflect on the stability margins of the input voltage controller. The objective of the input voltage controller is not to reduce these oscillations, but only to ensure that the total voltage is shared equally between the two converters. It may be observed that even in a single converter system the input voltage oscillations occur for a step change in input voltage.

2.4 Selection of gain, K

From the above discussion, it is clear that K should be at least higher than K_{\min} , and higher values of K result in faster correction in the input voltages after a disturbance. Comparing the plots Fig. 13 with different gains K , the peak overshoot in the input voltage (v_{in1} for the example considered) also decreases with higher values of K . However, higher K results in larger switch currents momentarily, during input voltage disturbances. Since, in most designs, MOSFETs are usually chosen with a significantly higher current rating than required (in order to reduce $R_{DS\ ON}$), it is possible to choose high values of K . The actual choice of K depends on the expected tolerances in the input capacitor values, the characteristic impedance of the input LC filter and the magnitude of disturbance expected in the total input voltage. The equivalent circuit of Fig. 7 will be useful in selecting appropriate value for K .

3. INPUT-SERIES AND OUTPUT-SERIES CONFIGURATION

A three-loop control scheme has been developed for the input series and output series (ISOS) configuration to ensure input and output voltage sharing under dynamic and steady state conditions [27]. The dynamic input voltage reference for the input voltage loop achieves minimum interactions among the different converters and among different control loops. Analysis based on incremental negative resistance characteristic of dc-dc converters, has been used to develop suitable design methods for the different control loops. It is shown that a proportional controller is sufficient for the input voltage loop. The proposed scheme has been fully validated through numerical simulation as well as through results from a 400 W hardware prototype.

3.1 Feasibility of ISOS scheme and need for dedicated input-voltage controller

The feasibility of the ISOS scheme in the presence of mismatches in different converter parameters (like turns-ratio of power transformer) is demonstrated using the concept of power balance, under steady state. Referring to Fig. 14, due to series connection at the input, the average input currents of the two converters are equal in steady state. Similarly, series connection at the output ensures that the average output currents of the converters are equal, in steady state. Further, if the input voltages of the two converters are also maintained equal *by control*, then the input powers, and therefore, by power balance the output powers, of the two converters will be equal. This automatically ensures that the converters share the output voltage equally.

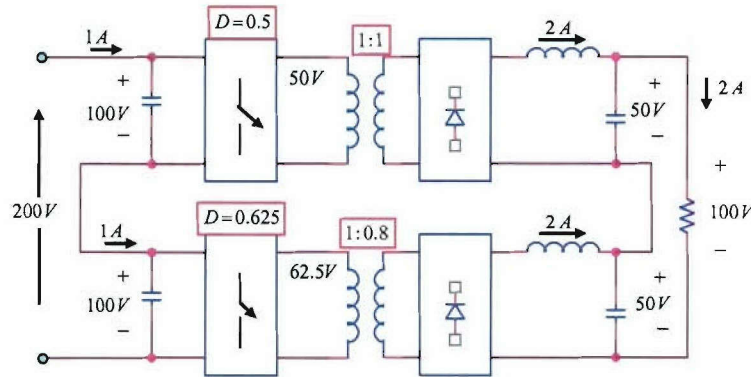


Fig. 14. Input and output voltage sharing with mismatched transformer turns-ratios.

For identical converters, the control applies equal duty ratios to the two converters. With differences in converter parameters, especially the turns ratios of the power transformers, the duty ratios of the two converters will be different, so as to maintain the ratio of individual converter output current to individual converter input current the same for both converters. This is illustrated in the numerical example of Fig. 14, where a 20% mismatch is introduced in the turns-ratios of the power transformers, in spite of which the converters share the input and output voltages perfectly equally. The above discussion applies to converters operating under both voltage mode control as well as current mode control, and can also be extended to any number of converters connected in series.

However, it is important to note that stable operation does not result when two standard, independent dc-dc converters, without any special control for sharing, are connected in ISOS configuration. In the absence of input voltage sharing control, any small disturbance causes a runaway of the converter input voltages due to the negative input resistance property of dc-dc converters. For example, if a small disturbance causes a converter input voltage to increase, its control loop reduces its duty ratio, thereby reducing the average input current. This results in further increase in the input voltage of the corresponding converter, ultimately leading to the entire input voltage appearing across this converter, as shown in Fig. 15.

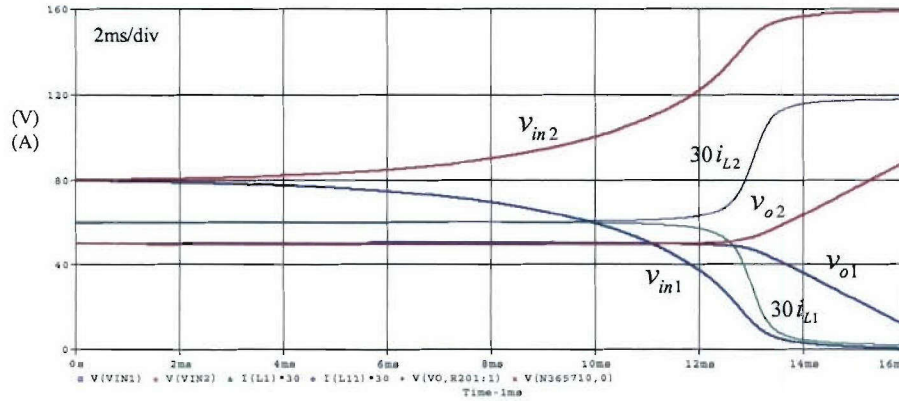


Fig. 15. Converter input voltages, output voltages and output inductor currents diverge, and run away in the *absence* of an input voltage control loop.

For ISOP connection, the common-duty ratio scheme, where the different converters are not controlled independently, but by a **common duty-ratio**, results in stable voltage and current

sharing [18, 20]. However, such a scheme does not work for the ISOS connection as explained below. Due to series connection at the output, the converter output currents need to be equal under steady state. With common duty-ratio control, a converter with slightly larger turns-ratio will tend to draw higher input current compared to the other converters. This is not possible under steady state, since the series connection at input mandates that input currents of all the converters be equal. Hence, a dedicated input-voltage loop, which changes the duty-ratios according to the mismatches in the different converter parameters such as transformer turns ratios, is required to ensure stable input and output voltage sharing.

From similar analysis, it can be shown that the common duty ratio scheme will result in stable operation for the ISOP and IPOS configurations, and unstable operation for IPOP and ISOS configurations. Table I gives the complete details related to the suitability of common duty ratio scheme for different modular configurations.

Table I – Suitability of common duty ratio scheme for the four combinations of input-output connections.

Mode	Stability	Output current	Output voltage	Input current	Input voltage
IPOP	Unstable	Converter with higher 'n' carries entire load current	Equal due to parallel connection	Converter with higher 'n' carries entire current	Equal due to parallel connection
IPOS	Stable	Equal due to series connection	Converter with higher 'n' has slightly higher voltage	Converter with higher 'n' carries slightly higher current	Equal due to parallel connection
ISOP	Stable	Converter with higher 'n' carries slightly lower current	Equal due to parallel connection	Equal due to series connection	Converter with higher 'n' has slightly lower voltage
ISOS	Unstable	Equal due to series connection	Converter with lower 'n' supports entire voltage	Equal due to series connection	Converter with lower 'n' supports entire voltage

3.2 Three-loop, dynamic input voltage reference control scheme for ISOS configuration

The dynamic input voltage reference scheme for controlling converters connected in ISOS configuration is shown in Fig. 2. It has a common output voltage loop that provides the current reference (i'_{ref}) for the inner current loops of the individual converters. Each individual converter, in addition to the inner current loop, also has an input-voltage loop that adjusts the above current reference, such that the converter input voltages are maintained equal.

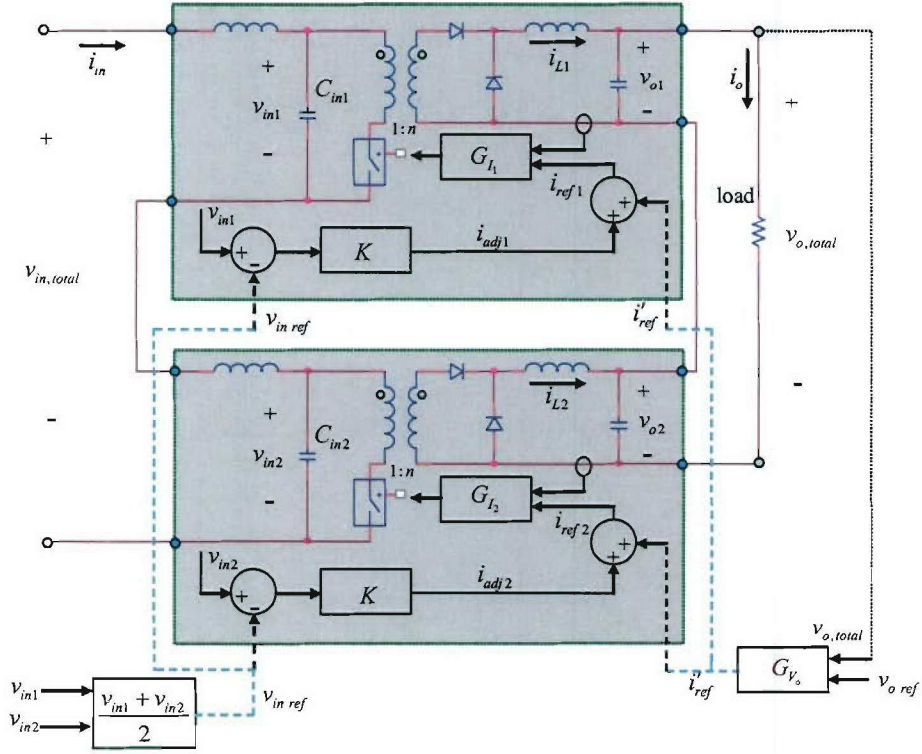


Fig. 16. Proposed control scheme for input-series, output series connection, corresponding to a two forward converter system. G_{V_o} and G_I are the gains of output voltage loop and inner current loops.

The reference for the above input-voltage loop in both the converters is the average of the two converter input voltages instantaneously, as given in (14).

$$v_{in,ref} = \frac{v_{in1} + v_{in2}}{2} \quad (14)$$

where, v_{in1} and v_{in2} are the instantaneous input voltages of the two converters, respectively. Clearly, this reference varies dynamically and includes the resonance due to the input LC filters.

For a general n converter system, the reference voltage is the average of all the converter input voltages. Similar to the ISOP configuration, this choice of reference results in **minimum interactions** among the converters and among the different control loops within a converter, as compared to other choices of reference such as $\frac{V_{in,total}}{n}$ or a constant reference. The minimum interaction is due to the unique property of the chosen reference that the sum of all correction currents (to correct for input voltage deviations) is zero, even under transients. Hence, the input voltage control does not affect the overall output voltage control loop.

3.3 Analysis and design criteria

In order to analyze the stability and performance of the input voltage control loop, the configuration shown in Fig. 16 can be represented by the simplified equivalent circuit illustrated in Fig. 17. This is identical to the model used for analyzing the ISOP connection as discussed Section 2. Due to the constant power characteristics of the individual forward converters, they can be represented by an equivalent incremental negative resistance connected to the input LC filter. The value of the negative resistance at full load is given by (2).

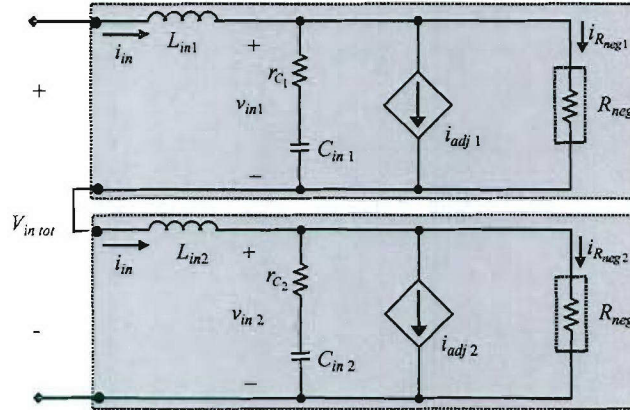


Fig. 17. Equivalent circuit for input voltage analysis of ISOS system.

The correction currents demanded by the input voltage control loop is actually realized by changing the output inductor current, and therefore the individual converter output voltage. However, assuming that the bandwidth of the output inductor current loop is much higher than that of the input voltage loop, the correction currents can be modeled as dependent current sources connected across the negative resistance model, as shown in Fig. 17. The value of this

current source, for example in converter 1, is given in (15), assuming a simple proportional controller of gain K for the input voltage loops.

$$i_{adj1} = K \left(\frac{v_{in1} - v_{in2}}{2} \right) \quad (15)$$

As the input voltage of a particular converter increases, the current drawn by the corresponding negative resistance decreases proportionately. A necessary condition for the stability of the input voltage loop is that the correction current, i_{adj} should be greater than the decrease in current in the negative resistance. This condition leads to the minimum value of gain, K_{min} given in (16), similar to the derivations done for the ISOP configuration in Section 2.

$$K_{min} = \frac{1}{n D_{min}} \frac{1}{R_{neg}} \quad (16)$$

where, D_{min} is the minimum duty-ratio and n is the turns-ratio of the power transformer.

The above value of K ensures stable operation, and higher values of K result in faster input voltage correction. However, higher values of K increase the magnitude of correction currents, and hence, the maximum value of K is constrained by the current ratings of the switches. The magnitude of the correction currents is significantly affected by the difference in the values of input filter capacitors, which also should be considered in selecting suitable K .

Since, the parameters of the modular converters are expected not to vary very widely, the design of compensators for the output voltage loop is similar to that of a single converter. The design of inner current loop, either peak current or average current mode, is also similar to that of a single converter. It may be pointed out that these simplifications are possible only due to choice of the dynamic input voltage reference for the input voltage loop, which ensures minimum interactions among the converters and different control loops.

3.4 Simulation results

The proposed scheme was simulated for the two forward converter system using PWM switch average model [26]. The turns-ratio of the transformers and the value of input capacitors (33uF and 66uF) were purposely made quite different for the two converters to demonstrate the effectiveness of the proposed control scheme.

Fig. 18 shows the individual converter input voltages and output inductor currents, corresponding to a step change in total input voltage, for two very different, but stabilizing values of gain, K . As seen, in both cases, the converters are stable, and share the voltages equally. Higher value for K leads to faster correction in the input voltages, but the correction currents flowing through the switches are also higher.

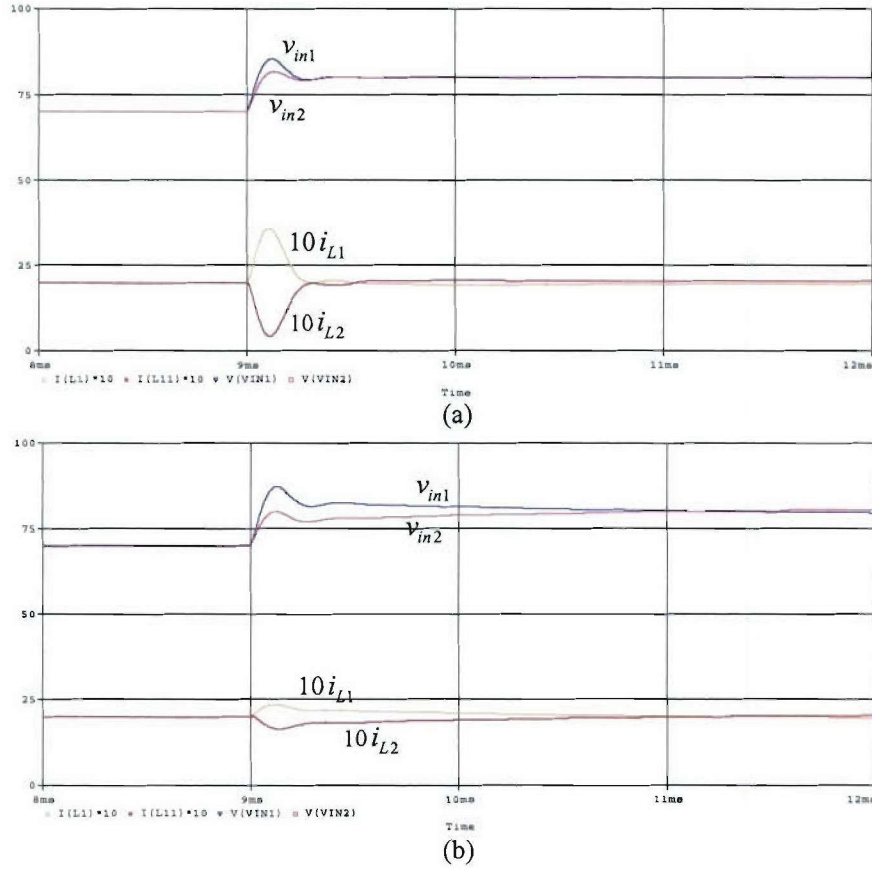


Fig. 18. Simulated individual input voltages and output inductor currents corresponding to a step change in total input voltage from 140V to 160V. (a) with $K = 20 \text{ Kmin}$ and (b) with $K = 2 \text{ Kmin}$.

Fig. 19 shows the total and individual output voltages, corresponding to the same step change in total input voltage. As seen, there is negligible effect on the total output voltage, though the individual output voltages change appreciably during the transient. This is one of the main advantages of the dynamic input voltage reference scheme.

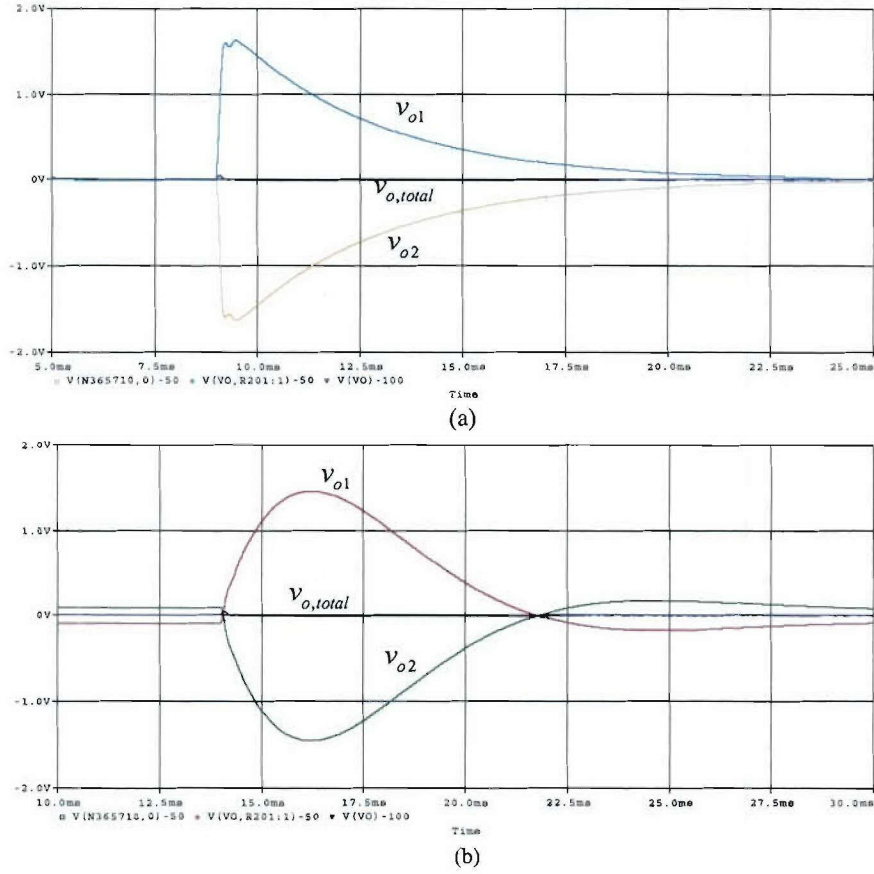


Fig. 19. Simulated individual output voltages and total output voltage corresponding to step change in total input voltage from 140V to 160V. Note that the voltages are in ac mode and the magnitudes highly expanded. (a) with $K = 20 K_{min}$ and (b) with $K = 2 K_{min}$.

3.5 Experimental results

The proposed scheme has been validated experimentally on proof-of-concept type prototype system with the following specifications.

Input voltage: 120 – 180V (shared equally by the two converters)

Output voltage: 100V (50V for each converter)

Maximum output current: 4A

Switching frequency: 200 kHz

The input voltages are sensed with magnetic isolation and peak current mode control is implemented for inner current loops of the two converters using UC2842A.

Fig. 20a shows the dynamic response in the input voltages of the two converters corresponding to a step change in total input voltage (from 140V to 160V). Note that this corresponds to a large difference - 1:2 in the values of input capacitors, chosen purposely. As seen, the converters share the input voltages well even under transient conditions. Fig. 20b shows the total output voltage, as well as the two individual output voltages (all in ac mode, to see the transients clearly), corresponding to the above step change in total input voltage. As seen, there is negligible effect in the total output voltage, since the changes in the individual output voltages cancel each other, a desirable characteristic of the dynamic input voltage reference scheme.

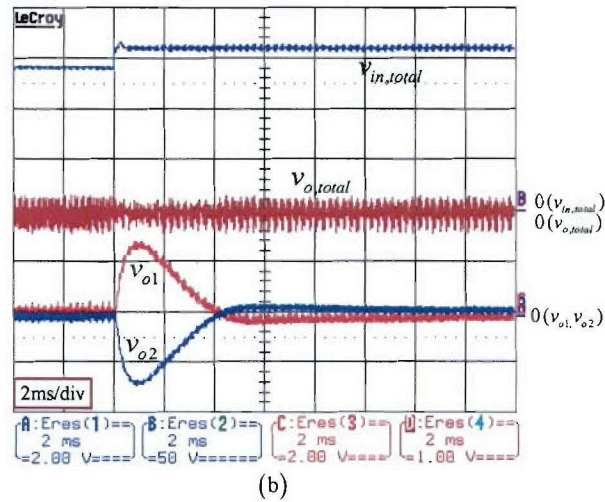
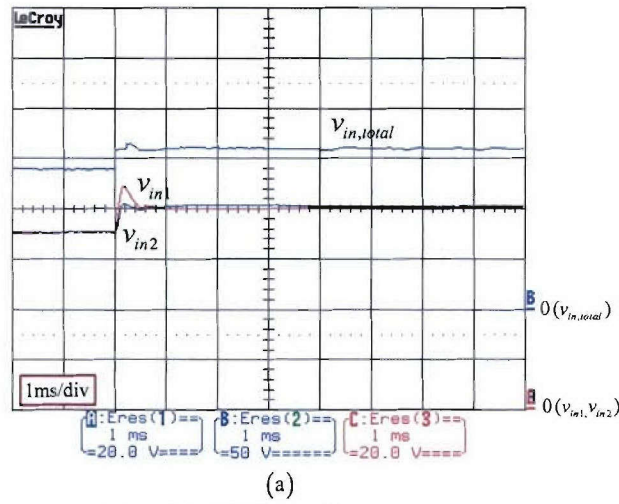


Fig. 20. Response to step change in total input voltage from 140V to 160V. (a) Individual converter input voltages and (b) total and individual output voltages (in ac mode).

Fig. 21 shows the two output inductor currents (averaged) corresponding to the step change in input voltage. As seen, the two inductor currents change momentarily to correct for the difference in the input voltages. It can also be seen that, the sum of the two inductor currents is equal to the total load current even during the transient.

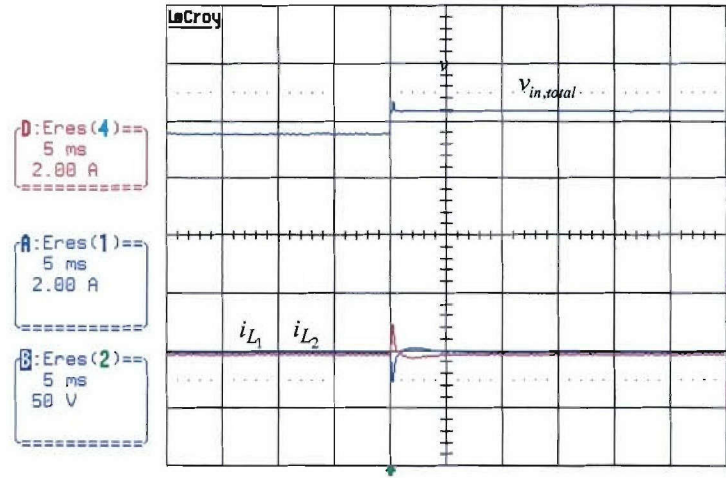


Fig. 21. Output inductor currents corresponding to step change in total input voltage.

Fig. 22 shows the output voltages, total and individual, corresponding to a step change in load current from 1A to 2A. As seen, the input voltage control loop does not affect the performance of the output voltage loop.

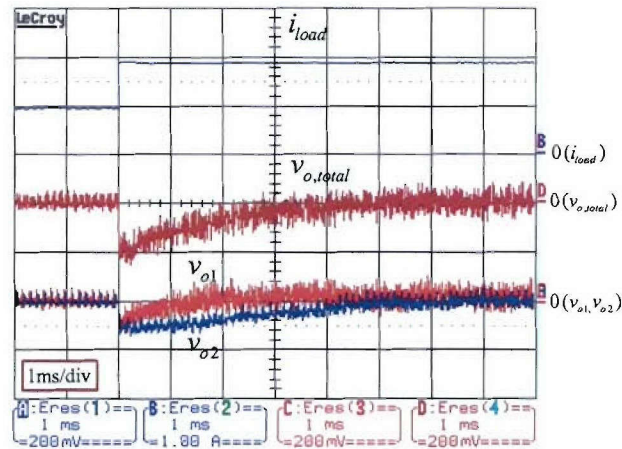


Fig. 22. Response in total and individual output voltages (ac mode) for a step change in load current.

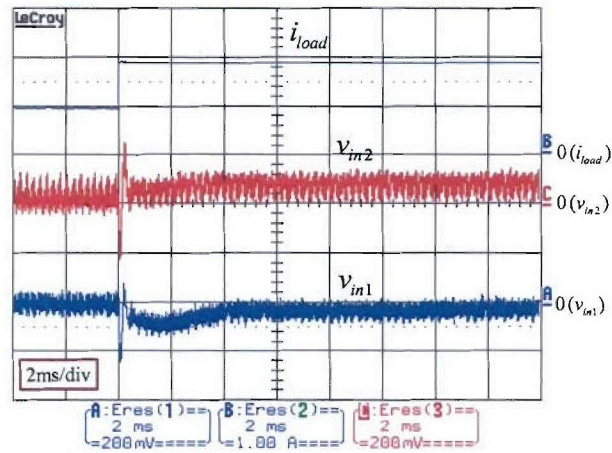


Fig. 23. Transient response in individual input voltages (ac mode) for a step change in load current.

Fig. 23 shows the individual converter input voltages, corresponding to the above step load change, and as seen there is very little effect on the input voltages (note that the waveforms are in ac mode, with a scale of 200mV/div).

3.6 Validation of the ISOS scheme on a *three* converter system

The dynamic input voltage reference scheme for the ISOS configuration has also been validated experimentally on a three-converter prototype with the following specifications.

Input voltage: 200 – 300V (shared equally by the three converters)

Output voltage: 144 V (48V for each converter)

Maximum output current: 4A

Switching frequency: 200 kHz

Fig. 24 shows the three individual output voltages (which are connected in series) in steady state. As seen, the converters share the output voltage equally at close to 45 V each. Fig. 25 shows the transformer secondary voltages for each of three converters. As seen, the converter with a slightly higher turns ratio (green waveform) automatically has reduced duty ratio such that the average of each of the waveforms during the ON interval (which is equal to the respective output voltage in steady state) ensuring sharing of the output voltage.

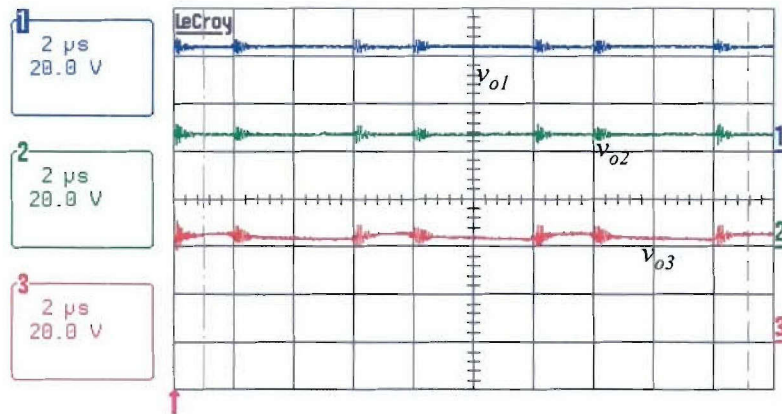


Fig. 24. Individual output voltages in steady state.

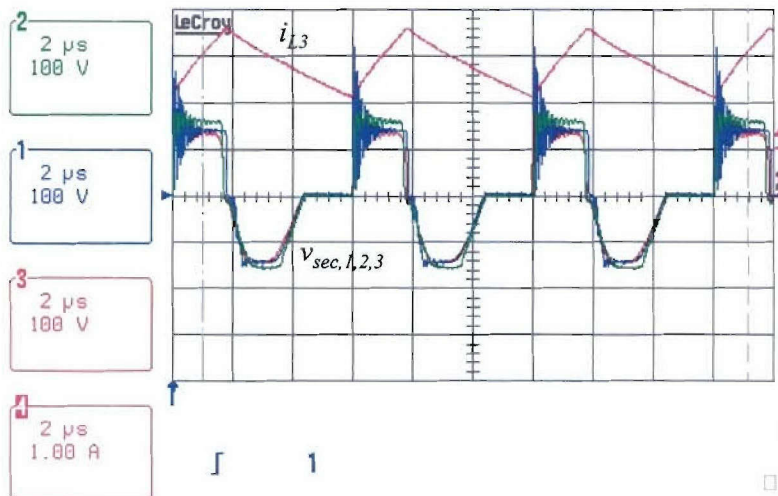


Fig. 25. Transformer secondary voltages for the three converters. One of the output inductor currents is also shown for reference.

Fig. 26 shows the dynamic response in the input voltages of the three converters corresponding to a step change in total input voltage from 250V to 280V. A large difference - 1:2 in the values of input capacitors was chosen purposely in order to study the effectiveness of the controller. As seen, the converters share the input voltages well under transient and steady state conditions.

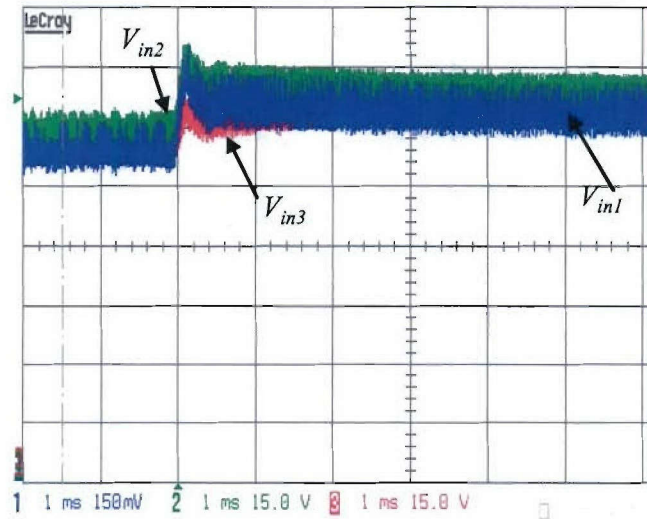


Fig. 26. Individual converter input voltages in response to step change in total input voltage from 250V to 280V (Scale: 15 V/div, 1ms/div).

4. MASTER LESS, AUTONOMOUS SCHEMES FOR ISOP CONFIGURATION

The schemes developed in earlier work for ISOP configuration, including the dynamic input voltage reference scheme and the common duty ratio scheme, required an output voltage control loop *common* to all the ' n ' converters. The module with this output voltage loop becomes the 'master' converter. Hence, the individual modules are not self-contained, and are not identical. This compromises the reliability of the system, since the failure of the master converter leads to the failure of the power system. In this research work, a master less scheme has been developed, where all the modules are identical and self-contained, with each module containing its own output voltage loop. This is achieved by the use of a novel "**input voltage share bus**" concept, inspired by the 'load share bus' concept used in conventional input parallel and output parallel (IPOP) configuration.

4.1 Input voltage share bus schemes

The input voltage share bus scheme for the autonomous ISOP configuration is shown in Fig 27. In this scheme, each module has its own dedicated control loop for output voltage regulation, similar to the load share bus schemes employed for load current sharing. In addition, each converter module has a dedicated input voltage control loop which suitably modifies the reference to the output voltage loop or the duty ratio directly, ensuring equal sharing of the input voltage. Once the input voltage of each converter is maintained constant, output load sharing is automatically ensured by the input series-output parallel connection. Fig. 27 shows a scheme corresponding to voltage mode control. The scheme is equally valid for the converters employing current mode control also.

Referring to the input voltage controller in Fig. 27, the input voltage of each converter (across the terminals of the input capacitor of each converter) is sensed and fed to a "K" block. The output of the "K" block of each converter is connected to an 'input voltage share bus' shared by all the converter modules. Depending on the structure of the "K" block, two different control schemes are possible (similar to the load share bus scheme). When the "K" block in each converter is a diode, a scaled version of the highest converter input voltage appears on the input voltage share bus. This leads to an "automatic master-slave active input voltage-sharing scheme", with the converter with highest input voltage becoming the 'automatic master'. In this

automatic master-slave approach, the input voltage of each converter is compared with the highest converter input voltage. The resulting error in each converter is amplified by the input voltage controller, and is used to adjust the output voltage reference of the particular converter. Hence, for example, if the input voltage of any converter reduces, its output voltage reference is also designed to reduce. This leads to reduction in the converter input current, thereby correcting for the reduction in converter input voltage.

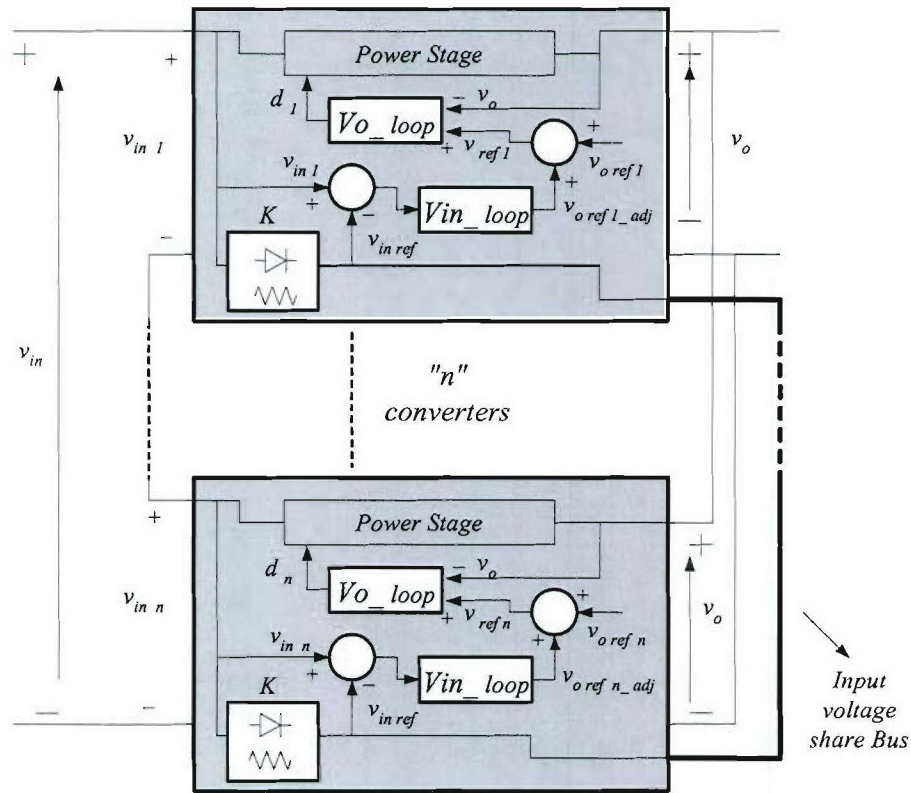


Fig. 27. Block diagram of the proposed 'input voltage share bus scheme' for ISOP converters. (Depending on whether the 'K' block is a diode or a suitable resistor, 'automatic master-slave scheme' or 'democratic voltage sharing scheme' is achieved, respectively.)

When the "K" block is a suitably designed resistor, the voltage at the input voltage share bus is proportional to the *average* of all converter input voltages, or $\frac{Vin_1 + Vin_2 + \dots + Vin_n}{n}$.

This leads to the "democratic active input voltage sharing scheme", where each converter input voltage is compared to a reference voltage that is proportional to the *average* of all the converter

input voltages. The resulting error signal, as in the previous scheme, is used to adjust the output voltage reference of each converter, thereby ensuring input voltage sharing.

In terms of performance, the democratic active input voltage sharing scheme is similar to the ‘dynamic input voltage reference scheme’ developed for master-slave configuration [18, 28]. Both the schemes result in fast dynamic performance, with little interaction among the various loops within a converter. The major advantage of the newly proposed ‘democratic input voltage sharing scheme’ is that the modules are all identical and self-contained, unlike the earlier work, where an external output voltage loop that was common to all the converters was needed.

The output signal of the input-voltage loop can be added at three different points in the system leading to three different control methods: (i) directly at the final duty ratio signal of a converter module, (ii) at the output voltage reference of each module and (iii) at the current reference signal of each module if current mode control is employed. From analysis and simulation it has been determined that the addition of input-voltage correction signal to the output voltage reference of each individual converter module, as shown in Fig. 27 results in the best performance, and hence is studied in detail in this work.

4.2 Current mode control versus voltage mode control for the ISOP converter modules

In the scheme discussed in Section 2 for the ISOP configuration, the input voltage sharing depended on directly controlling the output inductor current, and therefore, the current drawn from the input capacitor, in proportion to the input voltage difference. This was achieved by using converters with current mode control and suitably modifying the current reference for the individual converters depending on the error in input voltage sharing. As discussed in Section 2, current mode control with a common current reference for the modules, results in *unstable runaway condition*, if input voltage control is not implemented. This was due to the negative resistance characteristic of the individual converter module with current mode control. The design of the input voltage controller was based on overcoming this negative resistance as given in (9).

However, in the proposed master less scheme with input voltage share bus, the input voltage sharing can be achieved by adjusting individual voltage references instead of current references for inner current loops. In particular, the converter modules need not be current mode

controlled. A main advantage of the voltage mode control is that the absence of an input voltage control loop *does not necessarily result in a runaway condition*. The converter input voltages and individual load currents differ to the extent that the parameters of the output voltage controller and power stage parameters (like transformer turns ratios, resistances of various windings) are different. However, the critical parameter is the output voltage reference of the individual converters. Even small deviations in the references, for example 1% of the nominal value, can result in the duty ratio of the converter with higher reference voltage saturating at the maximum value, and leading to runaway of the input voltage and load current. Since, even the high precision voltage references within PWM IC's have small but finite tolerances, a dedicated input voltage control loop is still required (even if small mismatch in input voltage sharing proportional to mismatch in power stage parameters or controller parameters can be tolerated). However, unlike the current mode control designs where the input voltage controller needs to overcome the effective incremental negative resistance of the converter, here the input voltage controller needs to correct only for the mismatch in the voltage references for the output voltage control loop.

As in the previous schemes, a simple proportional controller is sufficient for the input voltage control loop. The minimum gain of the proportional controller is determined based on the maximum expected tolerance in the output voltage reference (usually less than 1%) and the allowable deviation in the input voltage sharing. Higher gain results in better sharing in the presence of errors in voltage references, as well as better dynamic performance. However, higher gain involves larger correction currents through the MOSFETs and diodes. Hence, upper limit on the gain of the proportional controller should be based on the expected tolerance in the input capacitance values, tolerance in the voltage references for the output voltage loop and the maximum current allowable through the MOSFETs, which are designed based on load current requirement.

4.3 Simulation of the democratic input voltage share bus scheme

The proposed democratic input voltage share bus scheme has been validated initially using numerical simulation corresponding to a system of two forward converters connected in ISOP configuration. The total input voltage is 200 V and the total load current is 8 A with an

output voltage of 50 V. The simulation uses the PWM switch average model for the two forward converters.

As discussed earlier, with voltage mode control, the ISOP configuration does not result in runaway condition for small mismatches in the parameters of the power stage such as transformer turns ratios or in the controller parameters. Fig. 28 shows the two individual converter input voltages and the individual load currents corresponding to a 10% mismatch in the transformer turns ratios, with other parameters and voltage references remaining identical for the two converters. A step change in the total input voltage from 170 V to 200 V is applied at 5 ms. The input voltage control is disabled for this simulation. As seen, the input voltages and the load currents are different to the extent the turns ratios are different. This condition is similar to the common duty ratio scheme [20], since with the controller parameters, output voltage and voltage reference remaining the same for the two converters, their respective duty ratios also remain the same. The converter with higher turns-ratio shares smaller input voltage and smaller load current.

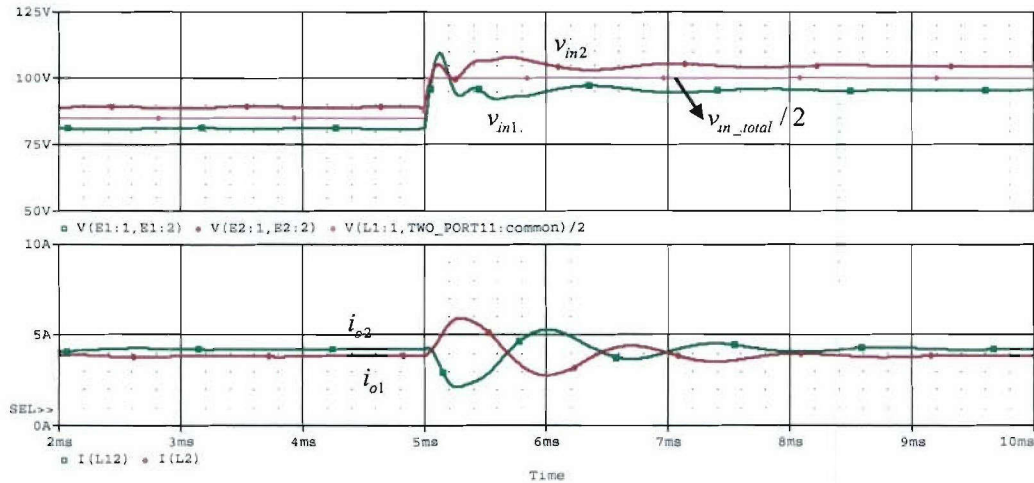


Fig. 28. Individual input voltages and output currents with mismatch in turns-ratio and without any input voltage controller.

Fig. 29 shows the simulation waveforms corresponding to a 20% difference in the gain of the output voltage controller. Again the input voltage controller is disabled. As seen, there is a mismatch in input voltage and load current sharing in proportion to the difference in the controller gains. But, the converters do not runaway with the full input voltage or load current.

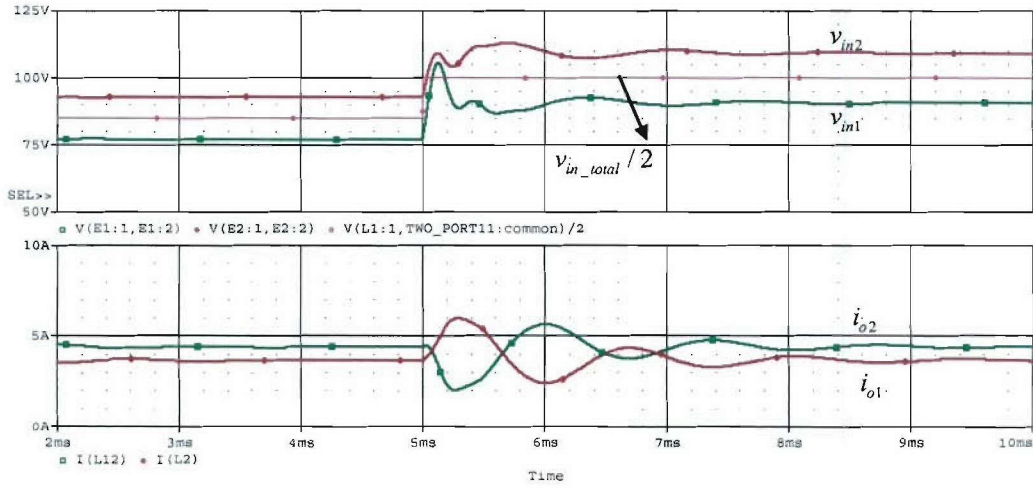


Fig. 29. Individual input voltages and output currents with mismatch in output voltage controller gains and without any input voltage controller.

Fig. 30 shows the simulation waveforms corresponding to a 2% difference in the output reference voltages for the two converters (converter 2 has higher reference), with all other parameters remaining the same for the two converters. As seen, converter 1 which has lower reference voltage runs away with the entire input voltage and the total load current. A smaller difference in the voltage references also lead to runaway condition, but with a proportionately longer time constant.

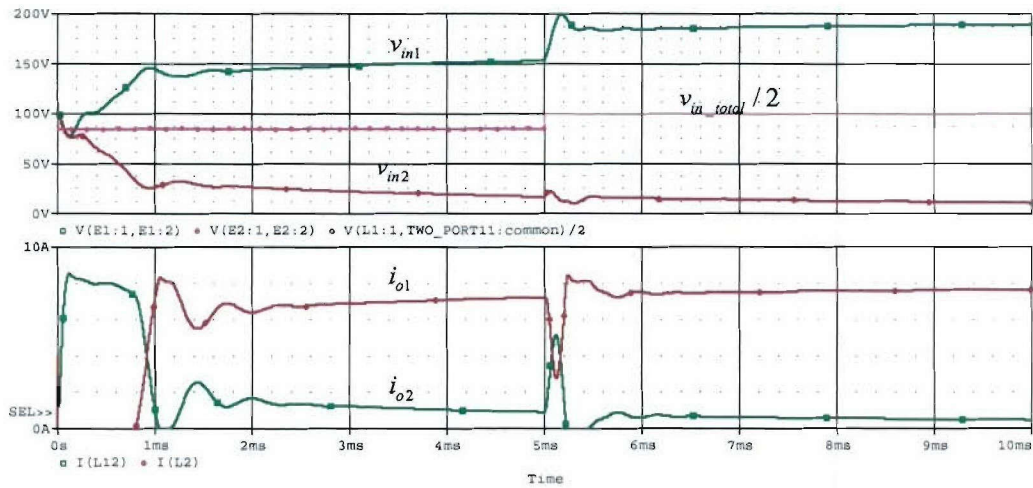


Fig. 30. Individual input voltages and output currents with a 2% mismatch in output reference voltage and without any input voltage controller.

Fig. 31 shows the waveforms corresponding to mismatch in transformer turns ratio as well a mismatch in controller gain, but with the input voltage controller enabled. As seen, the input voltage and load current are shared equally.

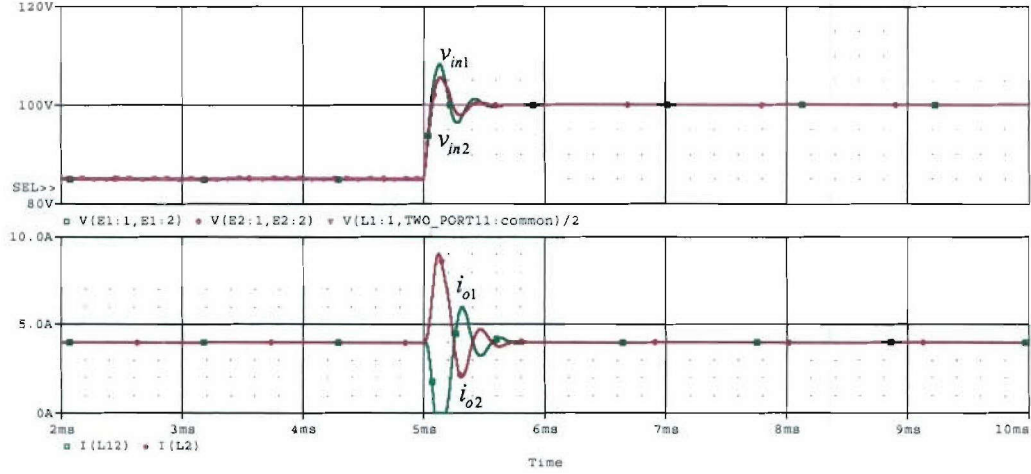
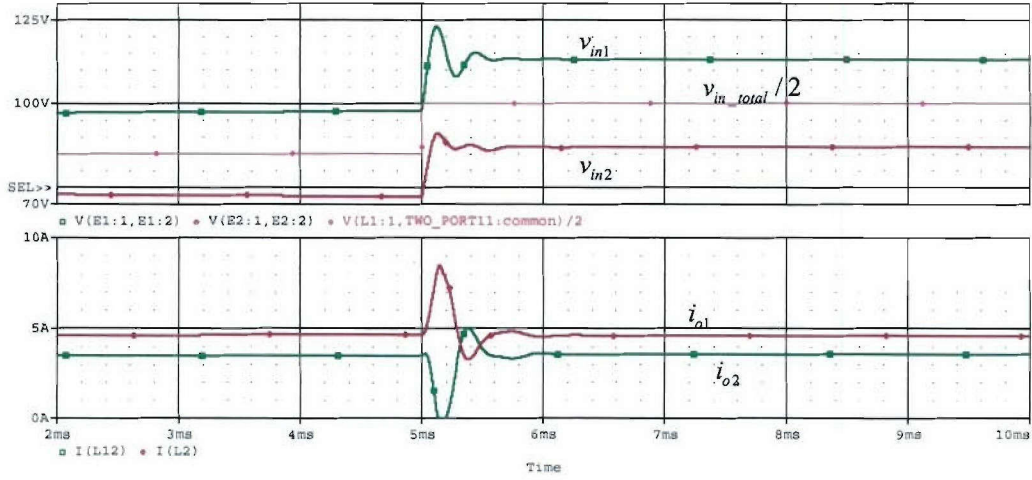
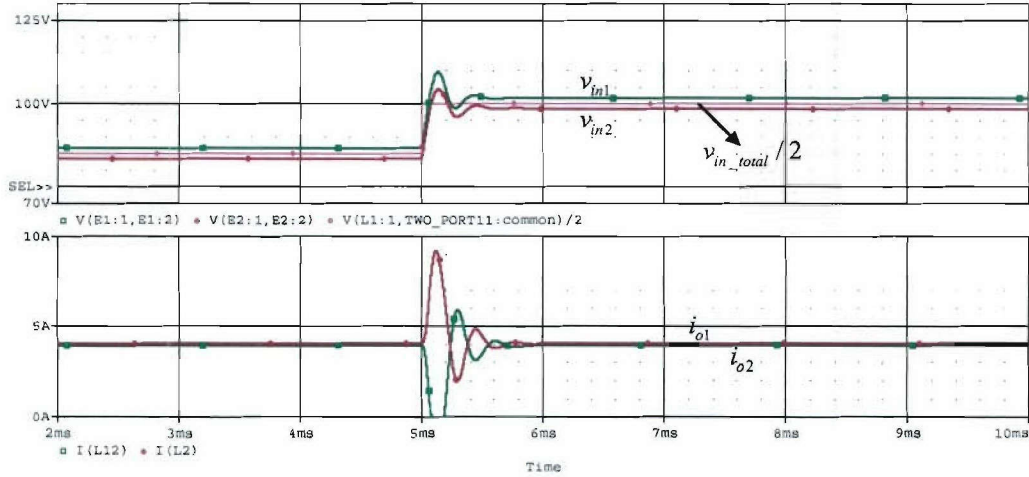


Fig. 31. Individual input voltages and output currents with mismatch in turns-ratios and output voltage controller gains, and with input voltage controller enabled.

Fig. 32 shows the waveforms corresponding to 2% mismatch in the output voltage references, with the input voltage controller included. Fig. 32a corresponds to a dc gain of 0.00326 in the transfer function from $(v_{in1} - v_{bus})$ to $v_{o1,ref}$. Fig. 32b corresponds to a larger dc gain of 0.0326. As seen, the operation is stable for both the gains, with a slight error in sharing that depends on the gain of the input voltage loop. For a 2% mismatch in the output voltage reference, the dc gain of 0.0326 in the input voltage loop results in less than $\pm 1.5\%$ error in the individual input voltages and output currents. For a 30 V step change in total input voltage and with 1:2 variation in the input capacitances, this gain results in the MOSFET current becoming twice the normal full load current. However, for a closer tolerance in the input capacitance values the corrections currents can be significantly smaller.



(a)



(b)

Fig. 32. Individual input voltages and output currents with a 2% mismatch in output reference voltage and with input voltage controller enabled. (a) with a dc gain of 0.00326 and (b) with a dc gain of 0.0326.

4.4 Experimental validation

The democratic input voltage share bus scheme has been implemented on a two-converter hardware prototype with the following specifications.

Input voltage: 150 – 200V (shared equally by the two converters)
 Output voltage: 48V
 Maximum output current: 10A
 Switching frequency: 200 kHz

The output signal of the input-voltage loop is used to adjust the output voltage reference for the individual converters as illustrated in Fig. 27. Each of the converter modules are voltage mode controlled. The input voltage is sensed through a transformer with a turns-ratio of 16:1.

Fig. 33 shows the individual input voltages and the output voltage in steady state. As seen, the input voltage is shared perfectly, with the democratic input voltage share scheme. Fig. 34 shows the steady state output inductor currents of the two converters demonstrating load current sharing. Here, the two converters are synchronized. However, the scheme does not require synchronization, and in particular, the converters can be interleaved to achieve ripple reduction.

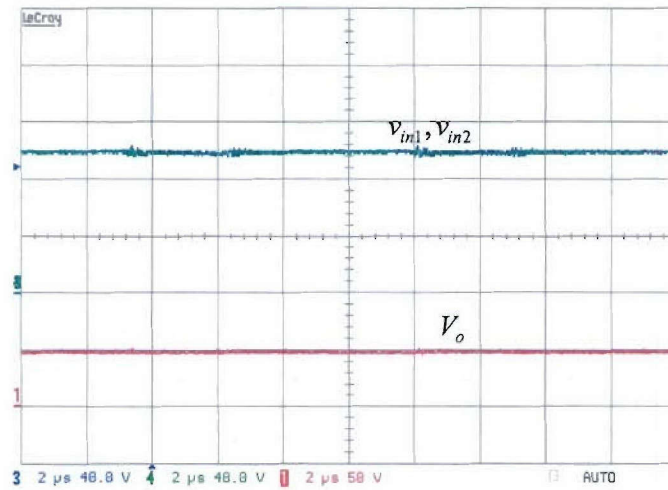


Fig. 33. Steady state input voltages and output voltage.

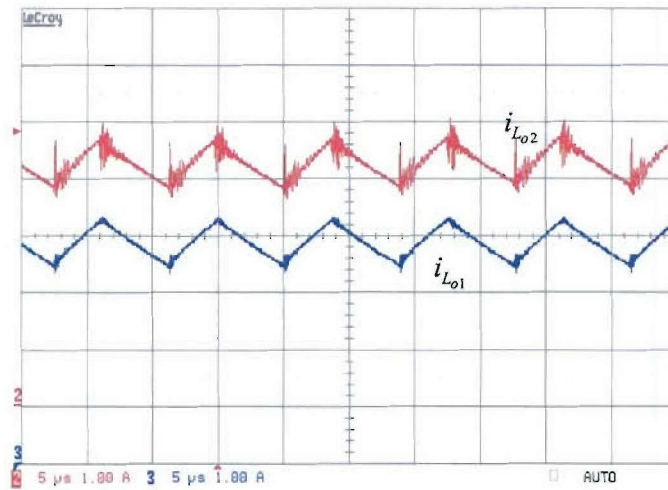


Fig. 34. Steady state output inductor currents.

Fig. 35 shows the transient individual input voltages corresponding to a step change in the total input voltage. As seen, the converters share the input voltage well during the transients also. Fig. 36 shows the two output currents corresponding to the above transient. The difference in the inductor currents during the transients corrects for the input voltage imbalance during the transient. Also, it may be noted that the sum of the two output currents is almost constant during the transient, resulting in negligible impact on the output voltage.

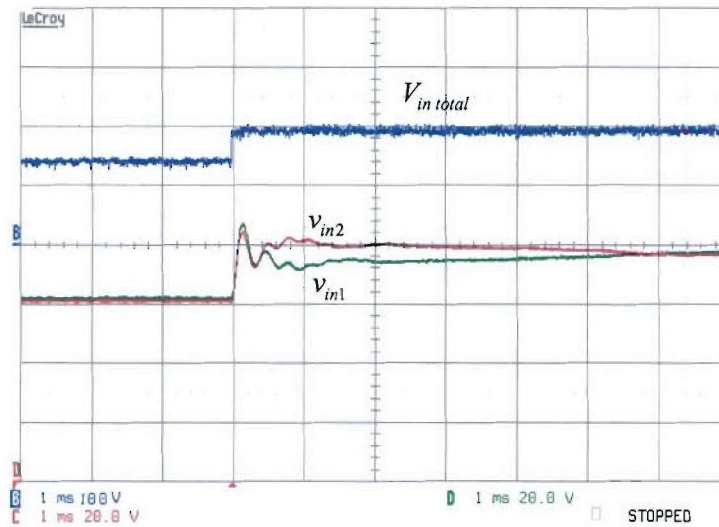


Fig. 35. Transient response in individual input voltages to a step change in total input voltage.

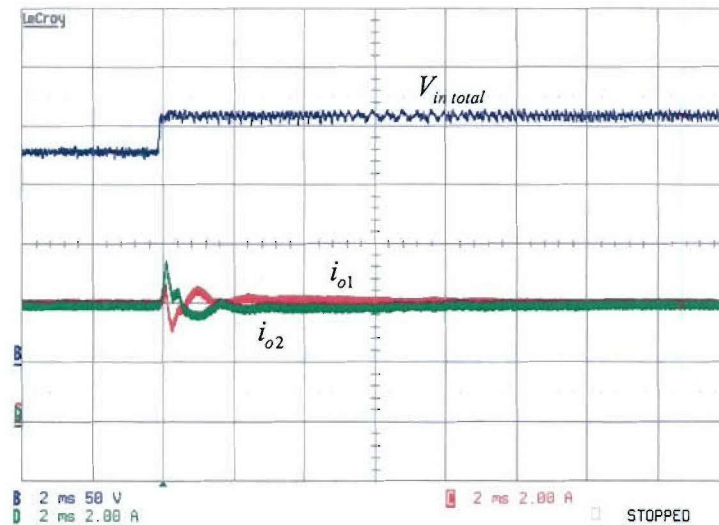


Fig. 36. Output inductor currents of the two converters in response to step change in total input voltage.

Fig. 37 shows the response in the output voltage due to step change in the load current from 4 A to 8 A with input voltage maintained at 200 V. Stable output voltage control loop with good phase margin, and negligible interaction with input voltage control loop can be inferred.

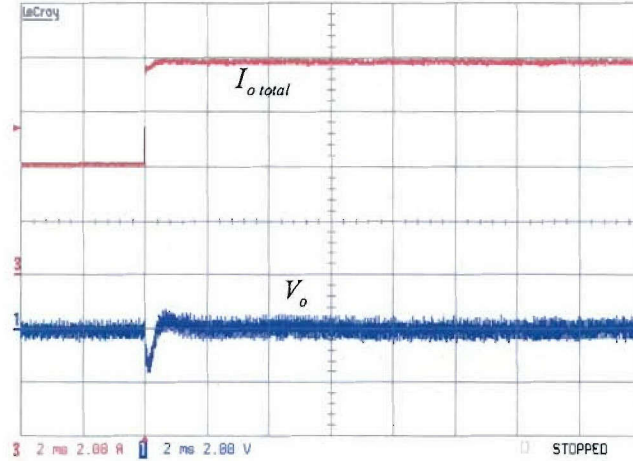


Fig. 37. Transient response in output voltage (ac mode) to a step change in load current.

Table I and II illustrate the input voltage and load current sharing performance of the prototypes corresponding to line and load variation respectively for the democratic share scheme.

Table II - Converter voltage sharing at a load of 8 A.

Vin-total (V)	Vin1 (V)	Vin2 (V)	Vo (V)
140	70.2	70.4	42.45
150	75.1	75.4	45.41
160	78.7	81.5	47.75
170	83.7	86.9	47.84
180	88.9	91.8	47.84
190	94.5	96.4	47.89
200	99.3	101.1	47.89
210	104.6	106.3	47.92
220	109.7	111.1	47.95
230	115.0	115.9	47.97
240	120.1	121.1	47.99

Table III - Converter load current sharing at total input voltage of 200V

Iload total (A)	Io1 (A)	Io2 (A)	Vo (V)
2	1.0	1.0	47.9
3	1.5	1.5	47.90
4	2.0	2.0	47.86
5	2.55	2.4	47.87
6	3.05	2.9	47.88
7	3.6	3.4	47.89
8	4.15	3.85	47.89

4.5 Fault tolerant capability with ISOP configuration

With self-contained and identical modules it is possible to design fault tolerant system with required amount of redundancy. In the event of failure of a module, it needs to be quickly isolated from the rest of the system, and the remaining healthy modules need to have sufficient rating to support the system. For the ISOP configuration, at the output side, the protection is similar to that employed in input-parallel and output-parallel configuration. However at the input side, if the switch fails open, then the input to the failed converter needs to be shorted. This provides an alternate path (instead of input capacitor of failed converter) for the input current to continue to flow and the rest of the system can share the total input voltage at a magnitude of $V_{in}/(n-1)$.

The fault tolerant capability of the proposed democratic share bus scheme has been validated using numerical simulation on a three-converter system. Fig. 38 shows the transient response in the individual input voltages to a step change in total input voltage from 300 V to 350 V. As seen, the input voltage is shared equally both during steady state and during the step transient. Fig. 39 shows the output voltage and the individual output currents. The output voltage has an overshoot similar in magnitude to that of a conventional voltage mode controlled single converter subjected to step input change. The individual output inductor currents are equal in steady state, and vary during the step change ensuring correction of input voltages.

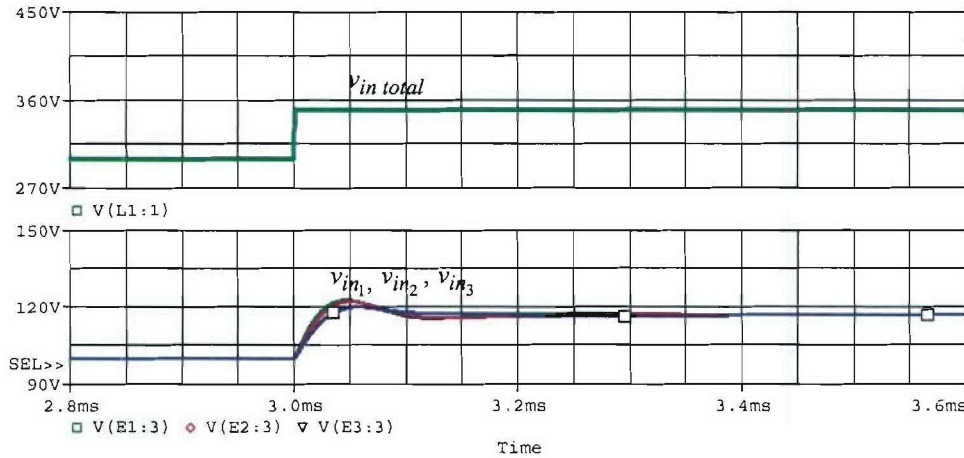


Fig. 38. Response in converter input voltages to step change in total system input voltage.

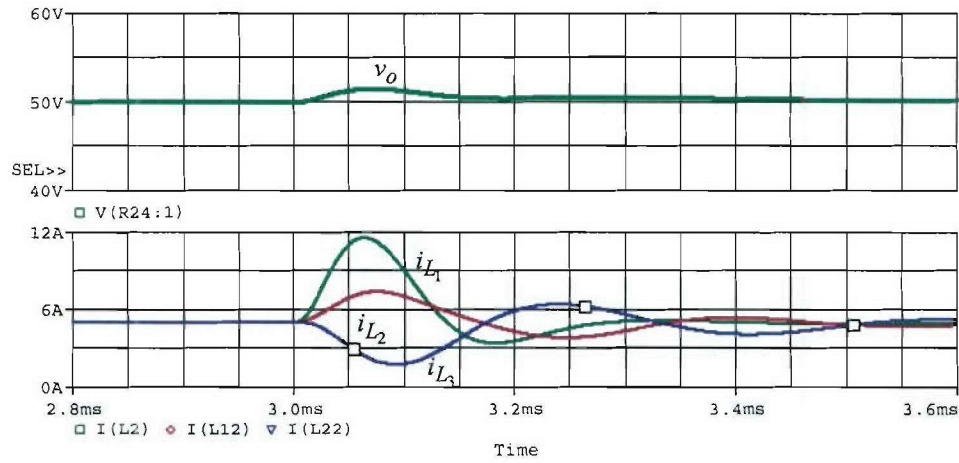


Fig. 39. Response in output voltage and individual output currents to step change in total input voltage.

In order to verify the fault tolerant capability with the democratic input voltage share scheme implemented, one of the converters is purposely shorted. This could represent either a short circuit fault at the input or a open circuit failure which leads to over voltage which is sensed and the particular converter shorted at the input. Figs. 40a to 40d show the corresponding waveforms of individual input voltages, duty ratios of each converter, output voltage and the individual output inductor currents respectively. As seen, the failed converter is isolated (shorted at the input), and the remaining two converters share the additional voltage and load current equally. The correction current required for this fault transient is very large - about four times larger than the load current. This is due to a very small number of modules in the system considered – failure of a single module in a three module system. However, in practical implementations, where a large number of converters (for example, ten and above) form the complete system, the failure of a single converter can be absorbed with correction currents that are less than the nominal load current.

It may be mentioned that a fault tolerant ISOP system with common duty ratio control scheme has been experimentally demonstrated on there-converter system as part of a NASA project [29]. A fast failure detection scheme has been developed. Each converter has an SCR switch at the input which shorts the converter in the event of an open circuit failure of the corresponding converter.

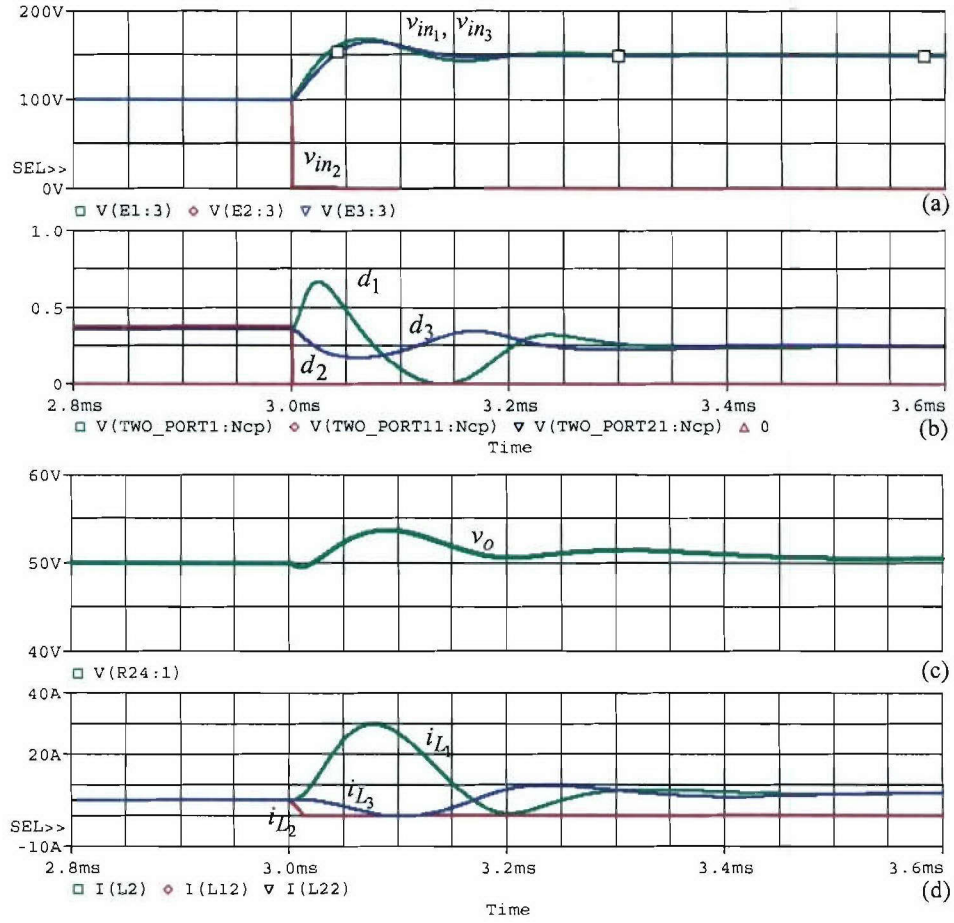


Fig. 40. Response to failure of a converter in a three-converter system (a) converter input voltages, (b) duty ratios of converters, (c) output voltage and (d) individual output currents.

4.6 Automatic-master-slave input voltage share bus scheme for ISOP configuration

Automatic-master-slave scheme is another modular scheme for ISOP connection using identical modules, and is realized when the K-block in Fig. 27 is implemented by diodes. All converter modules have independent output voltage loops and separate input voltage control loops. The reference for the input voltage loop is obtained from the input voltage share bus, whose signal corresponds to the highest input voltage among the converters. The converter with the highest input voltage becomes the automatic master converter, and as the operating

conditions change different converters may become the master converter. As before, the contribution of the input voltage control loop is added to the output voltage reference of individual converters. The performance of this scheme is similar to that of the democratic input voltage share scheme discussed in the previous section. Implementation of fault tolerant capability is easier with the automatic-master-slave scheme, since the diodes connecting to the voltage share bus automatically prevent the failed converter from possibly distorting the signal at the share bus.

The automatic master-slave scheme has been implemented on a two forward converter prototype and the corresponding experimental results are presented below. Fig. 41 shows the individual input voltages, total input voltage and the output voltage in steady state. As seen, the input voltage is shared well by the two converters.

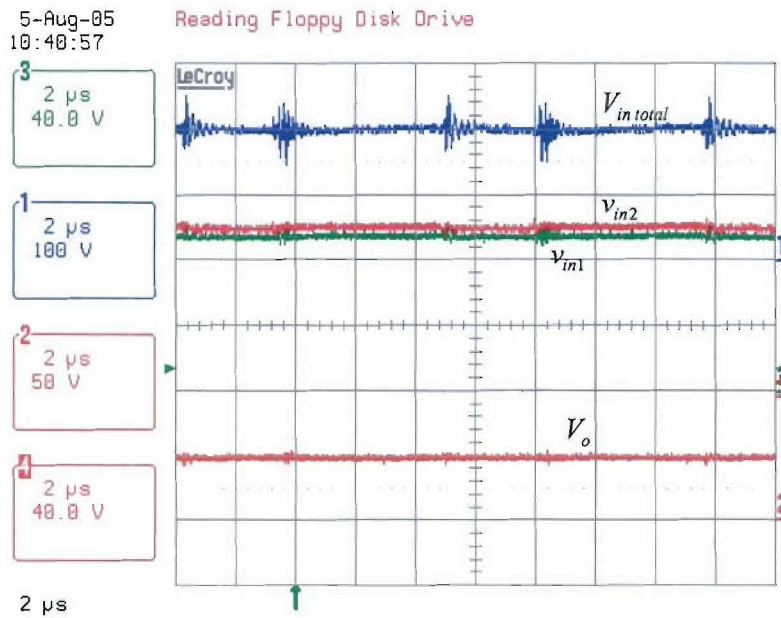


Fig. 41. Total input voltage, input capacitor voltages, and output voltage at full load for the automatic master-slave scheme.

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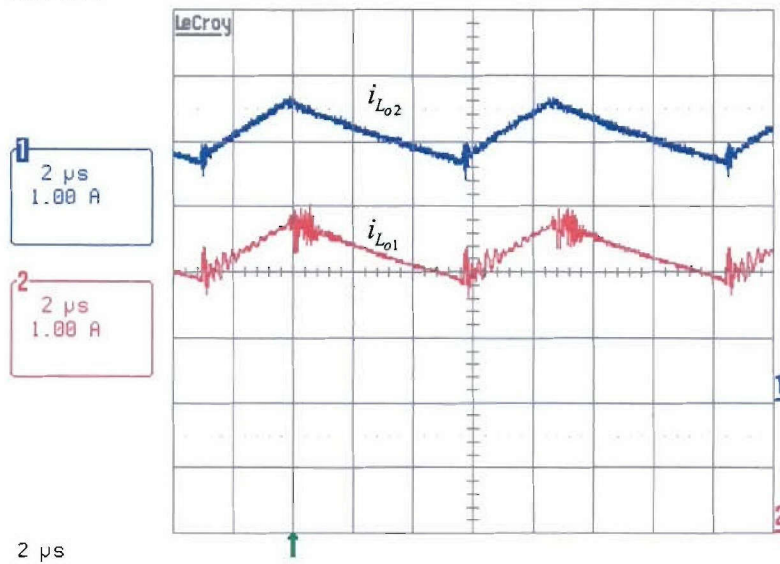


Fig. 42. Individual output inductor currents at full load.

Fig. 42 shows the steady state output inductor currents of the two converters at full load demonstrating load current sharing. Once again the converters are synchronized. Fig. 43 shows the transient individual input voltages corresponding to a step change of about 30 V in the total input voltage, demonstrating stable input voltage sharing.

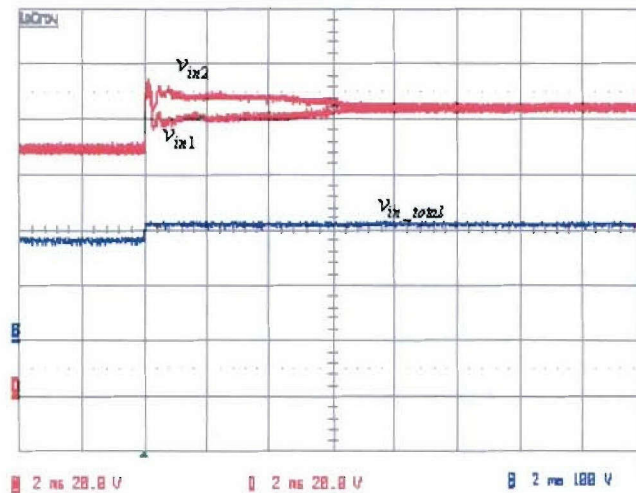


Fig.43. Transient response in individual converter input voltages for a step change in the total input voltage.

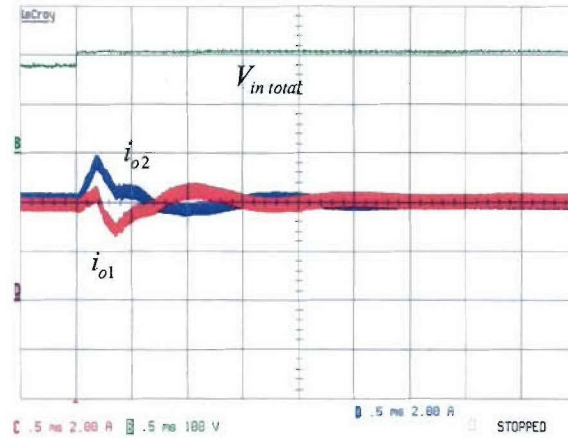


Fig. 44. Converter output currents for a step change in the total input voltage.

Fig. 44 shows the two output currents corresponding to the above transient. Again, the sum of the two output currents is almost constant during the transient, resulting in negligible impact on the output voltage. Table IV and Table V illustrate the input voltage and load current sharing performance of the prototypes under steady state, corresponding to line variation and load variation respectively.

Table IV - Converter voltage sharing at a load of 8 A.

Vin-total (V)	Vin1 (V)	Vin2 (V)	Vo (V)
140	70	69.45	42.5
150	74.5	73.97	45.2
160	79.65	79	47.8
170	85.25	83.7	47.9
180	90.6	88.36	47.39
190	95.9	93.1	47.9
200	99	99.8	48.1
210	104.3	104.7	48.1
220	109.5	109.5	48.1
230	114.2	114.9	48.1
240	118.6	120	48.1

Table V - Converter load current sharing at total input voltage of 200V

Iload total (A)	Io1 (A)	Io2 (A)	Vo (V)
2	1.0	1.0	48
3	1.5	1.5	48
4	2.0	2.0	48
5	2.55	2.45	48
6	3.05	3.09	48
7	3.6	3.4	48
8	4.2	3.8	48

5. MAGNETIC APPROACHES FOR INPUT VOLTAGE SHARING

A research task of this work is to investigate the feasibility of achieving input voltage sharing among modular converters, both under steady-state as well as during transients, using **magnetic coupling** between the input-series connected converters. A possible scheme for achieving active input voltage sharing and automatic load sharing of input-series, output-parallel converters, by magnetic means is shown in Fig. 45. As seen, each of the transformers of the individual forward converters has a separate input voltage balancing winding ('bal'), which are connected in a daisy-chain fashion to the following converter. With this arrangement, for example, if the input voltage across converter 1 increases compared to converter 2, then when S_1 is turned on, instantaneously diode D_{AB} will be forward biased, causing a correction current to flow from C_{i_1} to C_{i_2} , thus balancing the input voltages across the two converters.

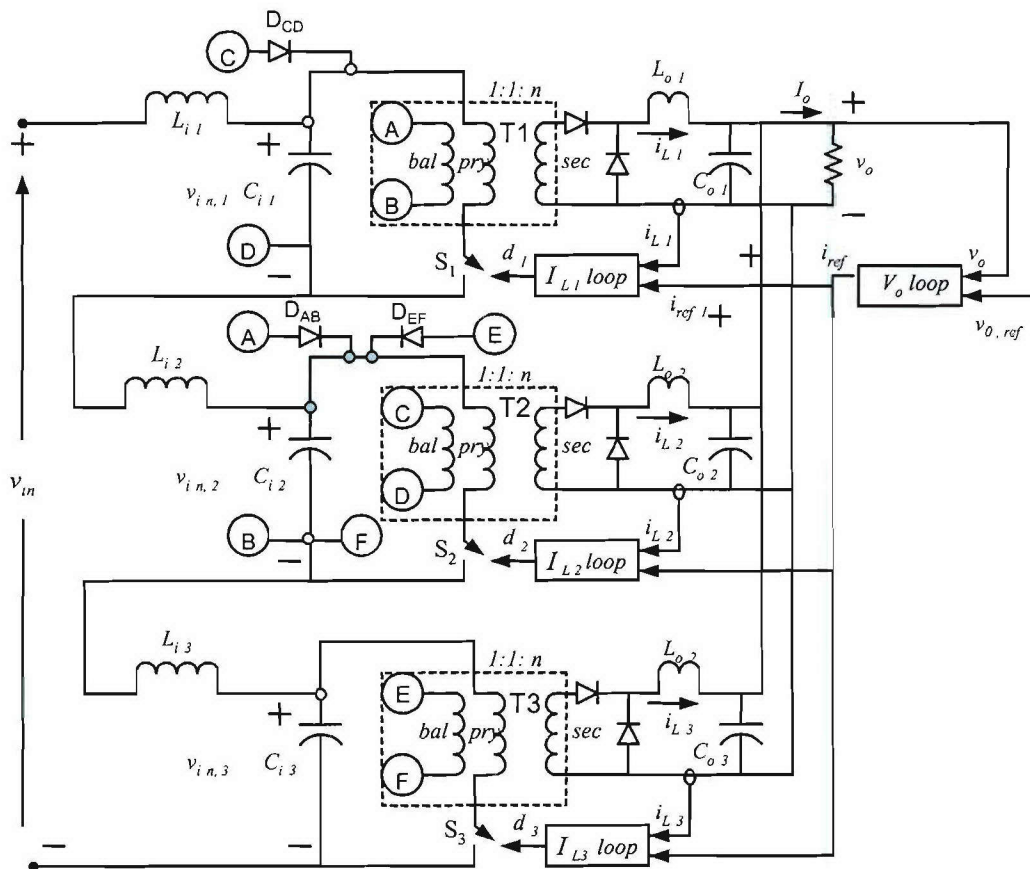


Fig. 45. Proposed scheme for input voltage sharing, using magnetic approach, among input-series connected modular converters.

The input voltage correction mechanism is independent of the control strategy adopted for the individual converters. In particular, there is no need for common control loops or any signal share buses that interconnect the converters. An objective of the research is to compare the advantages and disadvantages of the magnetic methods to those based on control methods in terms of steady-state and transient performances, overall power conversion efficiency, electromagnetic interference (EMI) and simplicity of implementation.

The scheme shown in Fig. 45 for achieving input voltage sharing and automatic load sharing of input-series, output-parallel converters by means of magnetic coupling was implemented in a hardware prototype comprising of two forward converters. The transformers of the individual forward converters have a separate input voltage balancing winding, which are connected through a diode to the other converter. Special efforts were done to minimize the leakage inductance of the balance winding. The input voltage control loop and input voltage share bus were disconnected, and the converters were connected in ISOP configuration.

However, the converters did not share the input voltage properly and showed a tendency to run away with full input voltage. The scheme was effective in simulation where the leakage inductance of the balance winding was made very small. However, even with careful winding implementation, the leakage inductance in the hardware prototype was too large for the scheme to be effective. Even under steady state, due to the large leakage inductance the balance current does not build up quickly to transfer the charges from the input capacitor of one converter to the other. Ideally, the balance currents were expected to be of very short pulses (less than 10% of the ON interval). However, in the hardware prototype the current pulses last for the entire ON interval and still do not complete the charge transfer leading to continuous build up of voltage in one converter. Fig. 46 shows the experimental waveforms of the balance current in one of the converters, its balance winding voltage and the input voltage of the other converter. As seen, the balance current lasts for the entire ON interval and continues to rise when the switch is turned off by control.

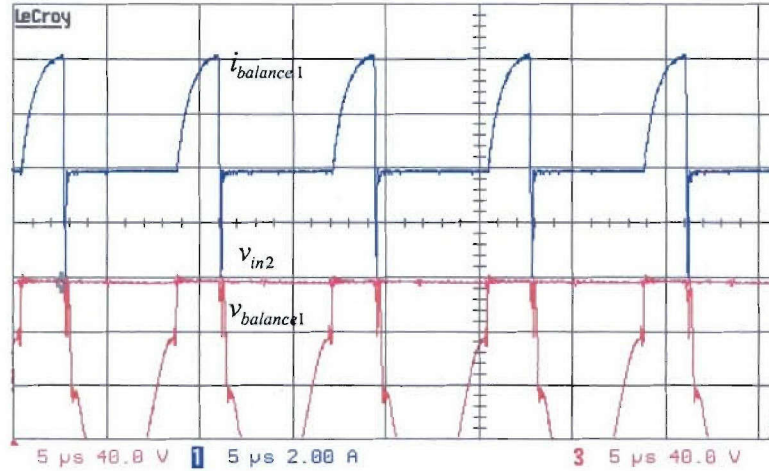


Fig. 46. Balance diode current, balance winding voltage and input voltage corresponding to the magnetic share scheme.

Also, note that the peak magnitude of the balance current is 4 A, which is comparable to the full load input current (about 5.6 A peak). The balance currents correspond to an input capacitance of 33 μ F. Lower values of input capacitance will result in smaller balance currents. Therefore, it is concluded that the magnetic means of achieving input voltage is not viable unless the leakage inductance of the balance windings as well as the value of input filter capacitance can be made very small. Even with small values of leakage inductance and input capacitance, another disadvantage of the magnetic method is that the balance currents continuously flow even during steady state and even when the converters share the input voltage in an average sense. Hence, it is concluded that the control based input voltage and load sharing methods are superior to the magnetic means.

6. INTERLEAVING TECHNIQUES FOR INPUT SERIES CONFIGURATIONS

One of the main advantages of the concept of modular converters is the possibility of significant reduction in the filter requirement, both at the input as well as at the output, by interleaving the converters. Interleaving refers to suitably phase shifting the clock signals of the various converters, such that the ripple currents in the individual output inductors and the ripple voltages in the individual input capacitors, cancel each other. Therefore, for a given system level ripple specifications, significantly smaller output and input filter inductors can be used. Apart from improvements in the power density of the power system and cost reduction, smaller filters also lead to improvements in the dynamic performance of the converter.

Filter reduction using interleaving techniques has been well studied for input parallel, output parallel converters [23]. This research project has investigated interleaving techniques for input-series and output-parallel converters. The interleaving at the output end (parallel connection) of ISOP configuration is identical to that of the conventional IPOP converters. Hence, the focus of this research has been on interleaving methods and performance evaluation *at the series connected input side*. Interleaving and ripple cancellation at the output is also briefly discussed to bring out the differences between interleaving of parallel converters vs. interleaving of series converters.

6.1 Interleaving and ripple reduction at the parallel connected output

Each of the converters are phase shifted by an angle of $360^\circ/n$, where 'n' is the number of interleaved parallel converters. At the output end of the ISOP configuration, as shown in Fig. 47, the sum of the currents through the individual output inductors flows through the load and the output capacitor. The dc components of the inductor currents add up to provide the dc load current. The switching frequency ripple components in the individual currents cancel to a certain extent and the effective (reduced) ripple current flows through the output capacitor causing the output voltage ripple. The frequency of the ripple current flowing in the capacitor is also multiplied by the number of interleaved parallel converters. The extent of cancellation in the ripple current depends on the number of converters and the operating duty ratio. When the duty ratio is exactly equal to $1/n$, the ripple currents cancel exactly, leading to zero ripple in their sum.

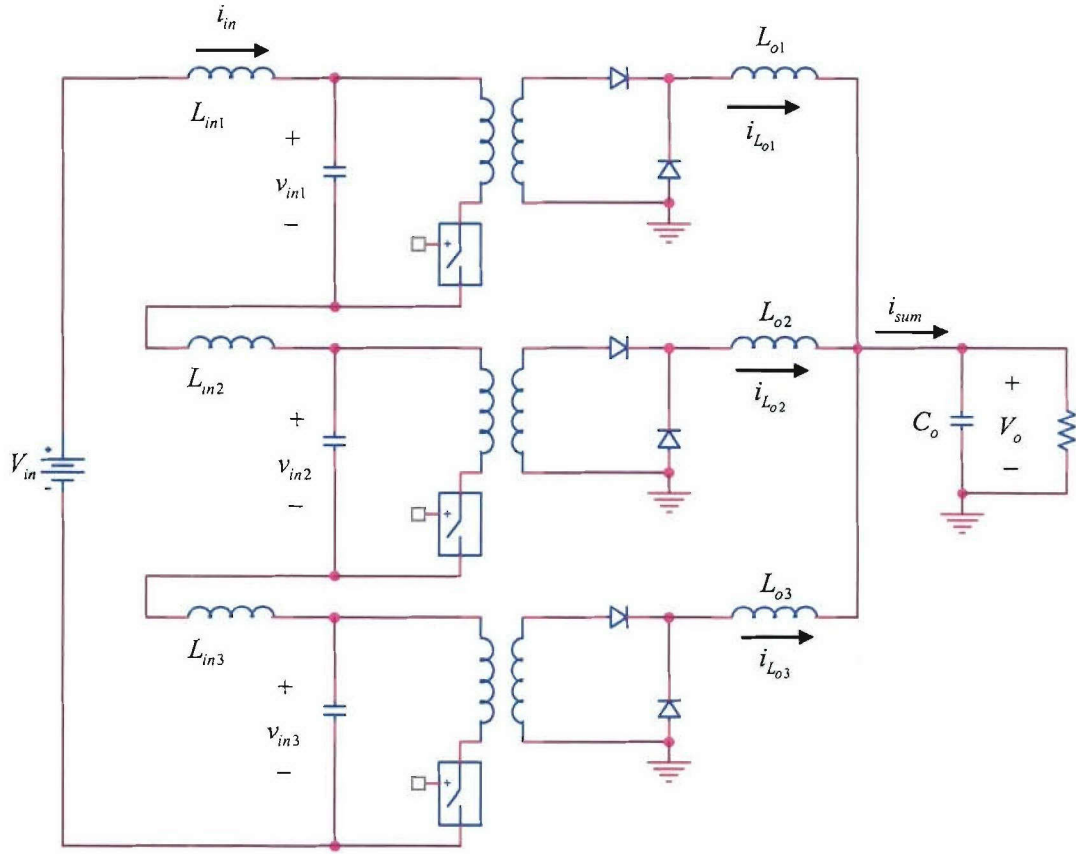


Fig. 47. ISOP configuration with three converters for interleaving analysis.

The standard design procedure for the output filter in a single, stand alone converter is to select the output inductor to limit its peak to peak ripple current to a specified value, for example 20% of the full load current, at the worst case operating condition. With this ripple current, the output capacitor is then chosen to meet the output voltage ripple (sum of ESR component and the capacitive component) specifications. A similar procedure is usually applied for the interleaved converters also. Due to ripple cancellation, the output capacitor can be significantly smaller. Alternatively, it is possible to trade off between the size of inductors and the size of capacitors.

6.2 Interleaving and ripple reduction at the series connected input

The standard procedure to design the *input filter* for a single, stand alone converter is to first select the input filter capacitor based on its maximum RMS current requirement considering

all the operating conditions. For a forward converter the RMS current through the input capacitor is given by (17).

$$I_{C,RMS} = I_o' \sqrt{D(1-D)} \quad (17)$$

where, I_o' is the load current reflected to the primary side of the transformer and D is the operating duty ratio. The capacitor is selected corresponding to the worst case operating condition (for which D is closest to 0.5) for the given specification. The voltage drop across the ESR of the capacitor is the main ripple voltage across the input filter inductor. The capacitive component of the ripple voltage is negligible compared to the ESR component.

Fig. 48 shows the current through the capacitor and the ripple voltage across the input filter inductor. The input inductor is designed to limit the ripple in the input current below the specified value. Therefore, the expression for the input inductance can be derived as given in (18).

$$L_{in} = \frac{I_o' D(1-D)(ESR)T_s}{\Delta I_{in}} \quad (18)$$

where, ΔI_{in} is the maximum peak-peak ripple in the input current and T_s is the switching period.

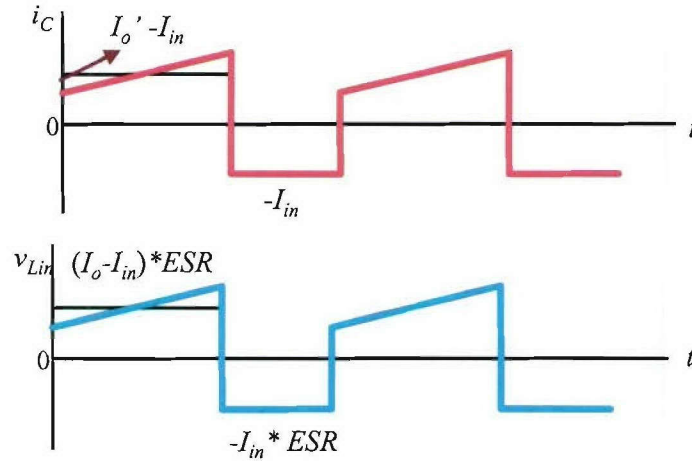


Fig. 48. Input capacitor current and ripple voltage across input inductor for a forward converter.

In the case of ISOP configuration where several converters are connected in series at the input as shown in Fig. 47, it can be seen that the capacitor current in each converter has the same waveform as that of a single converter as shown in Fig. 48, but phase shifted from each other. Hence, the RMS current through each of the input capacitors is the same as the single converter case. Therefore, the capacitor selection also remains unchanged from the single converter case. However, the phase shift introduces significant reduction in the ripple voltage applied across the input inductor. Referring to Fig. 47, the input inductors are all in series, and hence the input filter can be considered to be a single inductor (of value $n \cdot L_{in}$) and 'n' filter capacitors each across the input of the respective series connected converter. The ripple voltage across this equivalent, single inductor is the instantaneous sum of all the capacitor ripple voltages, which are phase shifted from each other. Due to ripple voltage cancellation due to phase shifting, the same input ripple current specification can be now met with a significantly smaller input filter inductor. Apart from size and cost savings, smaller input filter inductor is also advantageous from the view point of closed loop controller design [24].

Similar to the case of parallel connection at the output, for the input series configuration also the optimal phase shift among the modular converters is $360^\circ/n$. The following assumptions are made in order to analyze interleaving at the input. The total system output current, I_{o_total} is assumed constant, and 'n' converters share the total current equally. The total input voltage and output voltage are fixed. If more converters are present, then each has a lower module input voltage. The turns-ratio of the power transformer in each module, denoted by 'r' therefore varies with 'n' and without loss of generality it may be assumed that $r = n$. The specific values of V_{in} and V_o do not matter for this analysis. With I_{o_total} (and therefore, reflected individual converter current, $r \cdot I_{o_total}/n$) constant, the ripple in input current depends only on D , L_{in} and ESR of the input capacitors.

The capacitor selection is done based on RMS current rating, which is independent of 'n'. For the same RMS current rating, the ESR of the capacitor decreases with voltage rating but not exactly proportionately. However, in this analysis, it is assumed that the relationship is linear. Hence, the sum of the ESR of all capacitors remains the same for any 'n' and individual ESR is ESR_{total}/n . With this assumption, the inductance for each converter will also be proportional to its voltage rating (since ESR is proportional to voltage rating, and ripple current is required to

be the same). Therefore, the value of the equivalent single inductor also remains fixed. The analysis described below compares 'n' converters that are in phase with 'n' converters with interleaving, both the cases corresponding to ISOP configuration.

The input capacitor current can take one of two values:- $(I_o - I_{in})$ or $(-I_{in})$. For the case with no interleaving, all the converters have the same instantaneous value for the capacitor current, given by (19).

$$i_{c_j}(t) = \begin{cases} \text{if } 0 \leq t \leq DT_s \rightarrow (I_o - I_{in}) \\ \text{otherwise} \rightarrow (-I_{in}) \end{cases} \quad (19)$$

The ripple voltage across each input capacitor is the same and given by (20).

$$v_{c_j \text{ ripple}}(t) = i_{c_j}(t) \times ESR \quad (20)$$

The ripple voltage across the equivalent single input inductor is the instantaneous sum of the input capacitor ripple voltage, and is given by (21). For the in-phase or no interleaving case, this voltage is just n times the individual capacitor ripple voltage.

$$v_{L \text{ ripple}}(t) = \sum_{j=1}^n v_{c_j \text{ ripple}}(t) \quad (21)$$

The input ripple current is given by (22).

$$i_{in \text{ ripple}}(t) = \frac{\int_0^t v_{L \text{ ripple}}(t) dt}{L_{total}} \quad (22)$$

The above expressions are analyzed in MATHCAD with the following parameters: $T_s = 10 \mu s$, $I_{o_total} = 100 A$, $L_{in} = 100 \mu H$, $ESR_total = 1 \Omega$. The number of converters 'n' and the duty ratio, D are the variable parameters, with 'n' varying from 1 to 20 and D varying over the full possible range from 0 to 1.

The simulated waveform of the ripple voltage across the equivalent single inductor is shown in Fig. 49 and the input current ripple is shown in Fig. 50, both corresponding to $n = 5$ and $D = 0.25$.

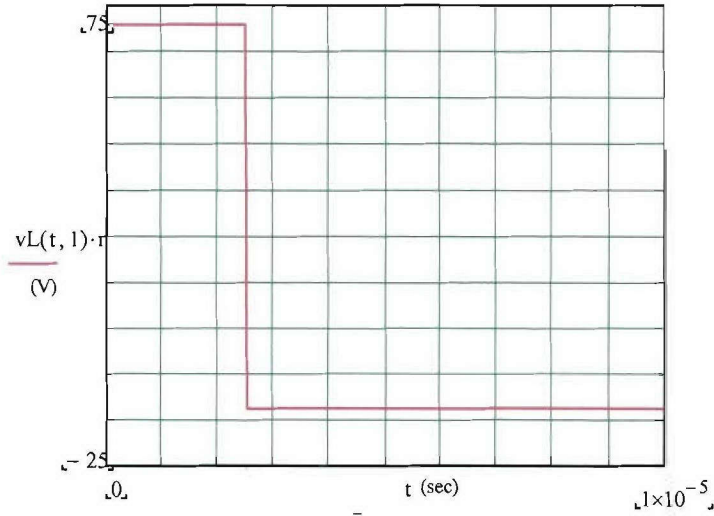


Fig. 49. Ripple voltage across the equivalent single input inductor for in-phase case with $n = 5$ and $D = 0.25$.

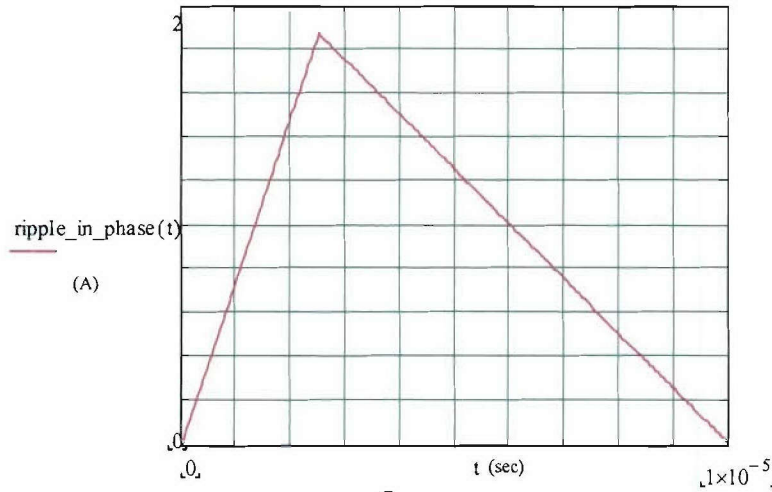


Fig. 50. Input ripple current the in-phase case with $n = 5$ and $D = 0.25$.

In the case of 'n' interleaved cases equations (20-22) are still valid. However, the expression for the individual capacitor currents is much more complex than that of the in phase case. In the interleaved case also the input capacitor current can take one of two values:- $(I_o - I_{in})$ or $(-I_{in})$. However, they are all not in phase, and the expression for the capacitor

currents need to take into account the number of converters and the duty ratio. The current through the input capacitor of the j^{th} converter is given in (23).

$$i_{C_j}(t) = \begin{cases} \text{if } \frac{(j-1)T_s}{n} \leq t \leq \left(D + \frac{j-1}{n}\right)T_s \rightarrow (I_o - I_{in}) \\ \text{otherwise} \rightarrow \begin{cases} \text{if } \left(\frac{j-1}{n} + D\right) > 1 \rightarrow \text{if } t \leq \left(\frac{j-1}{n} + D - 1\right)T_s \rightarrow (I_o - I_{in}) \\ \text{otherwise} \rightarrow (-I_{in}) \end{cases} \end{cases} \quad (23)$$

The simulated waveform of the ripple voltage across the equivalent single inductor in the case of interleaved configuration is shown in Fig. 51 and the input current ripple is shown in Fig. 52, both corresponding to $n = 5$ and $D = 0.25$ as in the previous case.

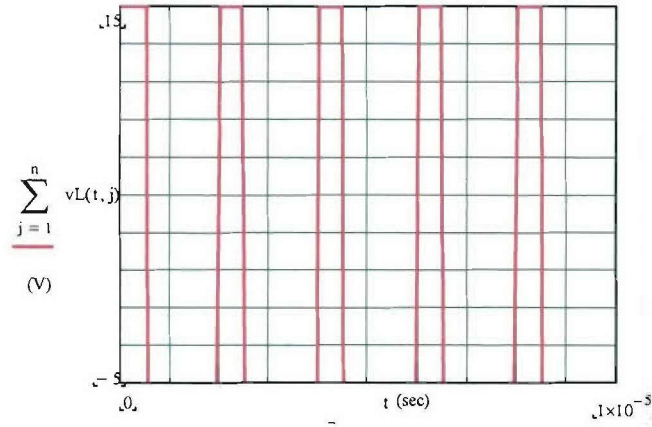


Fig. 51. Ripple voltage across equivalent single inductor for the *interleaved* case with $n = 5$ and $D = 0.25$.

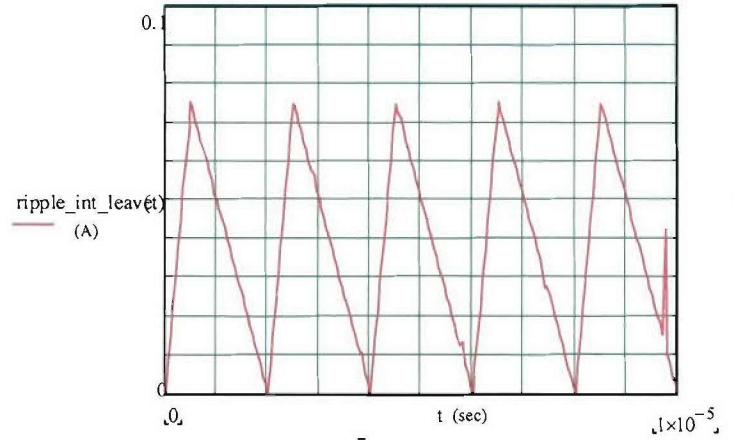


Fig. 52. Input ripple current for the *interleaved* case with $n = 5$ and $D = 0.25$.

As seen, the peak value of the inductor ripple voltage reduces by a factor of 5 and the frequency is multiplied by $n = 5$. Therefore, the peak-peak ripple in the input current reduces by a factor of 25. It may be noted that for $n = 5$, $D = 1/n = 0.2$ results in zero ripple in the input current. Since, the chosen operating duty ratio (0.25) is fairly close to the ideal value, the reduction in the ripple current, and therefore, in the inductor requirement is very significant.

The following analysis derives an analytical expression (instead of relying on generating time domain waveforms) for the peak-peak ripple in the input current as a function of 'n' and D .

Magnitude of the ripple voltage across the single inductor during the ON interval:

As seen from Fig. 51, the ripple voltage is at a frequency $n f_s$ where f_s is the switching frequency of each of the converters. The magnitude of this voltage during each of the 'n' ON intervals is calculated as below. At the start of the cycle, let x converters be ON and $(n - x)$ be OFF. So the total ON state current is given by (24).

$$\begin{aligned} \sum_{j=1}^n i_{C_j}(t) \Big|_{ON \text{ interval}} &= x(I_o - I_{in}) + (n - x)(-I_{in}) \\ &= xI_o - nI_{in} = I_o(x - nD) \end{aligned} \quad (24)$$

The number of converters, x that are ON at the start of the cycle can be shown to be equal to $ceil(nD)$. For example, with $n = 2$ and $D = 0.6$, the number of converters ON at the start of the cycle is $ceil(1.2) = 2$. Also, when nD is less than 1, there is no overlap of converters, and only the first converter is ON at the start of the cycle. Therefore, substituting the expression for x in (24),

$$\sum_{j=1}^n i_{C_j}(t) \Big|_{ON \text{ interval}} = I_o(ceil(nD) - nD) \quad (25)$$

The ripple voltage across the equivalent single inductor during the ON interval is given by,

$$v_{L \text{ ripple}}(t) \Big|_{ON \text{ interval}} = \sum_{j=1}^n i_{C_j}(t) \Big|_{ON \text{ interval}} \times ESR \quad (26)$$

Duration of the ON interval in Fig. 51:

In order to find the duration of the ON interval, the critical converter, which turns OFF first needs to be determined. From the analysis of the time domain waveforms, it can be shown that the critical converter k is given by (27).

$$k = n - (\text{floor}(nD) - 1) \quad (27)$$

The time at which the critical k^{th} converter is turned ON in the previous cycle is given by

$$k_{\text{start}} = \left[n - (\text{floor}(nD) - 1) - 1 \right] \frac{T_s}{n} = T_s - \frac{\text{floor}(nD) T_s}{n} \quad (28)$$

The duration of the ON interval in Fig. 51, defined as $T_{ON_interleaved}$ is the difference between the total ON duration of each converter (DT_s) and the ON time elapsed in the previous cycle for the critical converter, k . This duration is given in (29).

$$T_{ON_interleaved} = \left(D - \frac{\text{floor}(nD)}{n} \right) T_s \quad (29)$$

From (25), (26) and (29), the expression for the peak-peak ripple in input current can be derived as

$$i_{in_pk-pk} = (\text{ceil}(nD) - nD) \frac{I_o ESR}{L_{total}} \left(D - \frac{\text{floor}(nD)}{n} \right) \quad (30)$$

The normalized peak-peak ripple current with respect to the case of $n = 1$, and its worst case duty ratio of $D = 0.5$ is more useful for design purposes and is given in (31).

$$i_{in_pk-pk_norm} = \frac{(\text{ceil}(nD) - nD) \left(D - \frac{\text{floor}(nD)}{n} \right)}{0.25} \quad (31)$$

Fig. 53 shows the plot of the normalized peak-peak ripple current as a function of the duty ratio for various values of 'n'. As seen, ripple reduces significantly with 'n', and the frequency of the current is scaled by 'n'. Also, each of the plots has zero ripple current at $D = 1/n$.

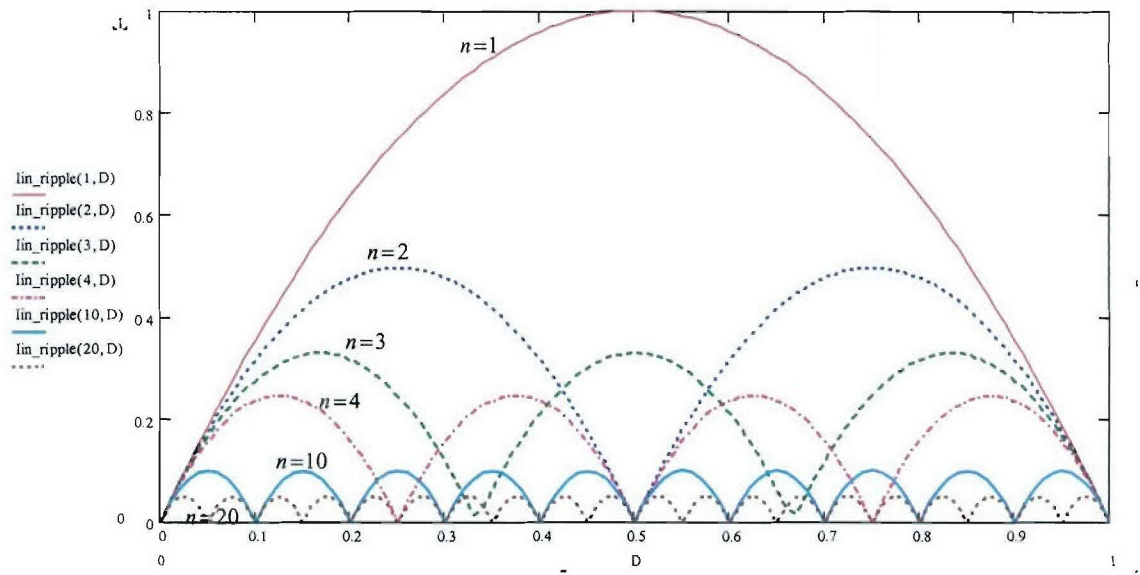


Fig. 53. Normalized input ripple current versus duty ratio for different number of interleaved converters for the ISOP configuration.

7. CONCLUSIONS

A fully modular power system architecture for dc-dc conversion, where low-power, low-voltage (input and output) building block dc-dc converters can be connected in any combination, series or parallel, both at the output *as well as at the input* sides, has several advantages including increased reliability, standardization of design and components, higher power density and efficiency. Though the input parallel combination of modular dc-dc converters has been well developed, work on input series combinations has been relatively few. Input series configurations are essential to realize a fully modular system, and also feature several other advantages apart from modularity. This research project has made significant contributions to the understanding of modular, autonomous input series configurations.

This project has explored the input-series and output-series (ISOS) configuration for the first time. The ISOS configuration is required for a fully modular dc-dc power system architecture and is especially useful when both the input and output voltages are high. A three-loop control scheme has been developed, which ensures input and output voltage sharing under dynamic and steady state conditions. The dynamic input voltage reference for the input voltage loop achieves minimum interactions among the different converters and among different control loops. Analysis based on incremental negative resistance model of dc-dc converters leads to suitable design methods for the input voltage control loop. A simple, proportional controller is sufficient for the input voltage loop. The proposed ISOS scheme has been fully validated through simulation as well as on a three-converter hardware prototype, and the results have been presented in this report.

An earlier ONR sponsored research work had developed control schemes for input-series and output-parallel (ISOP) configuration. However, all the schemes developed, required an output voltage control loop *common* to the ‘n’ converters. Hence, the individual modules were not self-contained, and were not identical, leading to degradation of modularity and reliability. The present project has developed autonomous control schemes that realize a fully modular system with self-contained and identical converter modules. In particular, each of the converter modules has its own dedicated output voltage control loop. These schemes make use of an input voltage share bus which either has the average of the input voltages of all the converter modules

leading to democratic share scheme or the highest input voltage of all the converter modules leading to automatic master-slave scheme. In both schemes, the individual input voltage is compared with the signal at the input voltage share bus. The error is used to adjust the output voltage reference of the respective module, thereby ensuring sharing of input voltages.

It has been found that voltage mode control with small mismatches in power stage parameters or controller parameters, unlike current mode control, does not result in a runaway condition. However, even very small differences in the output voltage reference obtained using PWM ICs, can lead to runaway conditions or very large mismatch in the input voltage and load current sharing. The input voltage loop with a proportional controller ensures equal sharing even in the presence of mismatches in the output voltage references as well as in any power stage parameters. Design methods to choose the gain of the input voltage controller have been developed. The analysis and design methods have been validated using numerical simulation and on a hardware prototype comprising of two forward converters. Since all the modules are identical, it becomes possible to introduce fault-tolerant capability. With appropriate ratings of the converter modules, the power system can safely withstand the failure of a few modules without any adverse effect.

Apart from the control-based schemes discussed above, this project also explored the possibility of input-voltage sharing in series connected converters through magnetic coupling among the converter modules. A possible advantage is the simplicity of implementation, since there is no need to sense the converter input voltages across isolation barriers. In the proposed scheme, the transformers of the individual forward converters have separate input voltage balancing winding, which are connected in a daisy-chain fashion to the following converter. Any imbalance of input voltages is to be corrected through the balance windings when the appropriate MOSFET turns on. However, for practical values of leakage inductance of the balance windings and typical values of input filter capacitances and switching frequency, the balance current does not build up quickly enough to transfer the charges from the input capacitor of one converter to the other. Also, the magnitude of the balance currents is comparable to that of the load current. The balance current continues to flow even when the input voltage is shared equally in an average sense. Hence, it is concluded that the control based approaches to input voltage and load sharing are superior to those that rely on magnetic coupling to achieve sharing.

A main advantage of series/parallel connection of modular converters, apart from standardization and reliability through redundancy, is the reduction of filter requirement through interleaving of the converter modules. Interleaving refers to suitable phase shifting of the gate drive signals of the modules such that there is significant cancellation of ripple in the input/output currents and/or voltages. Interleaving techniques for the parallel connections have been well studied. This project has investigated interleaving techniques for input series configurations. For the ISOP configuration, interleaving at the output end (parallel connection) is identical to that of the conventional IPOP converters. At the series connected input side also the optimal phase shift is $360^\circ/n$. At the input side, the current through the input capacitor is similar to that of a stand alone forward converter, and hence, there is no savings in the ratings of the input filter capacitor. However, the ripple voltages in the filter capacitors (which appear as the ripple voltage across the input inductor) cancel due to interleaving, leading to significant savings in the input inductor. The frequency of the ripple in the input current is scaled up by the number of converters. The savings in the filter requirement for various values of 'n' and duty ratio have been derived.

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